Design, Construction and Performance of The BELLE Silicon Vertex Detector

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Abstract

The primary goal of the BELLE experiment (KEK B-Factory) is observation and precise study of CP violation. In order to observe indirect CP violation in B meson system, measurement of the distance between the decay vertices of B and $\bar{B}$ mesons is necessary.

We constructed a dedicated detector for precise measurement of decay vertices, the Silicon Vertex Detector (SVD). The SVD was designed to achieve vertex resolution better than 100 μm, which is needed to measure CP violation parameters efficiently. Radiation hardness of frontend system was also considered. The SVD was successfully constructed and its performance was measured to satisfy the requirements.

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Chapter 1

Introduction

1.1 CP Violation

Various symmetries play very important role in particle physics. Some of them are continuous and the others are discrete. CP symmetry is one of the latter and the origin of its violation is one of the most exciting mystery in present particle physics. As its name indicates, CP transformation is product of two discrete operations, P and C.

Parity, P, is a symmetry of space. P invariance means that the mirror image of an experiment yields the same result as the original. Charge conjugation, C, is a symmetry between particle and antiparticle. C invariance means that experience in a world of antimatter will give identical results to the ones in our (of course, matter) world.

Until 1956, it was believed that all elementary processes are invariant under P and C. Lee and Yang pointed out the possibility of the violation of these symmetries, and subsequent experiments proved that P and C symmetries are really not conserved in weak interactions. However, the products of P and C transformations, CP was still a good symmetry.

The second impact came in 1964. An experiment using neutral K meson showed that CP is also not conserved under weak interactions[1]. Neutral K mesons (K^0 and $\bar{K}^0$) are created under strong interaction. The mass eigenstate of the $K^0 - \bar{K}^0$ system can be written

$$|K_S >= p|K^0 > +q|\bar{K}^0 >, |K_L >= p|K^0 > -q|\bar{K}^0 > \tag{1.1}$$

(choosing the phase so that $CP|K^0 >= |\bar{K}^0 >$). If CP invariance held, we would have q = p so that K_S would be CP even and K_L would be CP odd. Because kaon is the lightest strange meson, it decays through weak interaction. Neutral kaons can decay into two or three pions. Since pion has CP eigenvalue of -1, K_S always decays two pions and K_L decays into three pions, if CP is conserved in weak interactions. The experiment performed at Brookhaven[1] proved that a small faction of K_L decays into two pions, which means CP is violated in weak interaction. In kaon system, the order of observed CP asymmetry is $\sim 10^{-3}$.

1.2 Kobayashi-Maskawa Matrix

In 1973, Kobayashi and Maskawa proposed a theory of quark mixing which can introduce CP asymmetry within the framework of the Standard Model[2]. They demonstrated that quark mixing matrix with measurable complex phase introduces CP violation into interaction.

In the Standard Model, quark-W boson interaction part of Lagrangian is written as

$$L_{qW} = \frac{g}{\sqrt{2}} \left\{ \bar{u}_L \gamma^\mu W_\mu^+ \mathbf{V} d_L + h.c. \right\} \tag{1.2}$$

where g is weak coupling constant, u_L (d_L) represents left-handed component of u-type(d-type) quarks, and $\mathbf{V}$ is a quark-mixing matrix.

If all the elements of quark mixing matrix $\mathbf{V}$ are real, the amplitudes for a certain interaction and that for CP conjugate interaction are the same. In order to violate CP, $\mathbf{V}$ should have at least one complex phase as its parameter.

In general, N dimensional unitary matrix has N^2 parameters, with $N(N-1)/2$ real rotation angle and $N(N+1)/2$ phases. Since we can rephase quark fields except one relative phase, $(2N-1)$ phases are absorbed and $(N-1)^2$ physical parameters are left. Among them, $N(N-1)/2$ are real angle and $(N-1)(N-2)/2$ are phases. The presence of phases means some of the elements must be complex and this leads to CP violating transitions.

For the case of $N = 2$, two quark-lepton generations, there is 1 rotation angle (the Cabbibo angle) and no phases. This means CP must be conserved in the model with four quarks.

For three generations, $N = 3$, there are three rotation angles and one phase so that CP can be violated without altering the interaction. The quark mixing matrix for six-quark model can be written in many parameterization, but two parameterizations are especially well known.

$$\mathbf{V} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \tag{1.3}$$

$$= \begin{pmatrix} c_{12}c_{13} & s_{12}c_{13} & s_{13}e^{-i\delta_{13}} \\ -s_{12}c_{23} - c_{12}s_{23}s_{13}e^{i\delta_{13}} & c_{12}c_{23} - s_{12}s_{23}s_{13}e^{i\delta_{13}} & s_{13}c_{13} \\ s_{12}s_{23} - c_{12}c_{23}s_{13}e^{i\delta_{13}} & -c_{12}s_{23} - s_{12}c_{23}s_{13}e^{i\delta_{13}} & c_{23}c_{13} \end{pmatrix} \tag{1.4}$$

$$\simeq \begin{pmatrix} 1 - \frac{1}{2}\lambda^2 & \lambda & A\lambda^3(\rho - i\eta) \\ -\lambda & 1 - \frac{1}{2}\lambda^2 & A\lambda^2 \\ A\lambda^3(1 - \rho - i\eta) & -A\lambda^2 & 1 \end{pmatrix} \tag{1.5}$$

The first parameterization, (1.4) is by Particle Data Group, where $c_{ij} \equiv \cos\theta_{ij}$ and $s_{ij} \equiv \sin\theta_{ij}$ for $i = 1, 2, 3$.

The second parameterization(1.5), originally by Wolfenstein, is also widely used. It clearly indicates the hierarchy in the size of elements, the diagonal elements are almost unity, the elements between adjacent generations are smaller by an order of magnitude and the elements with the first and the third generations are further smaller. Setting λ to the sine of the Cabbibo angle, $\sin\theta_C \simeq 0.22$, and writing down all the elements in terms of powers of λ, the remaining three parameters are intended to be of order unity.

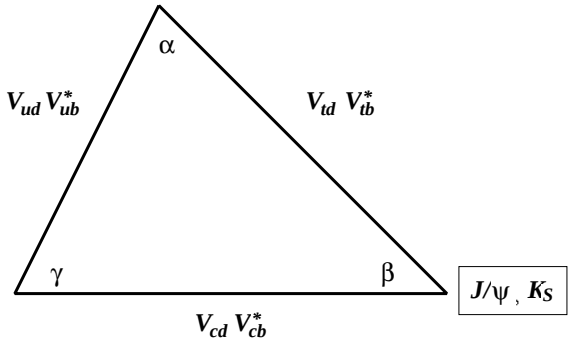

Figure 1.1: The Unitarity Triangle. The three angles are defined as $\alpha \equiv \arg\left(\frac{V_{td}V_{tb}^*}{V_{ud}V_{ub}^*}\right)$, $\beta \equiv \arg\left(\frac{V_{cd}V_{cb}^*}{V_{td}V_{tb}^*}\right)$ and $\gamma \equiv \arg\left(\frac{V_{cd}V_{cb}^*}{V_{ud}V_{ub}^*}\right)$

The unitarity of KM matrix leads to some constraints on its elements. For example, the first and second columns lead to the equation

$$V_{ud}{V_{us}}^* + V_{cd}{V_{cs}}^* + V_{td}{V_{ts}}^* = 0 \tag{1.6}$$

which is related to K meson system. Since the elements of KM matrix are complex, this implies they form triangles on a complex plane. Although the unitarity of KM matrix leads to six triangles, most of them have one side which is much shorter than the other two sides, and consequently one tiny angle. By Wolfenstein prametrization, one can compare the magnitudes of three terms in equation 1.6:

$$O(\lambda) + O(\lambda) + O(\lambda^5) = 0 \tag{1.7}$$

This explains why observed CP asymmetries in K decays, related to the tiny angle, are very small ($\sim 10^{-3}$).

On the other hand, B meson system is related to following equation:

$$V_{ud}{V_{ub}}^* + V_{cd}{V_{cb}}^* + V_{td}{V_{tb}}^* = 0 \tag{1.8}$$

where all the three terms are the same order of magnitude, $O(\lambda^3)$. This implies that all the three angle can be large in the triangle related to equation 1.8, which leads to the possibility of large observable CP asymmetries in B meson decays. The triangle related to B (illustrated in figure 1.1) is sometimes called as *the* "Unitarity Triangle".

Since only two generations are related to tree diagrams of K meson decays, the sensitivity to parameters related to CP violation is limited in K system. In B meson system, all the angle α, β and γ can be measured independently, which leads to precise tests of the Standard Model.

1.3 Measuring CP Asymmetry in B Meson Decays

B mesons can be produced in two energy regions, a center-of-mass energy equal to the $\Upsilon(4S)$ mass or a higher center-of-mass energy in the continuum.

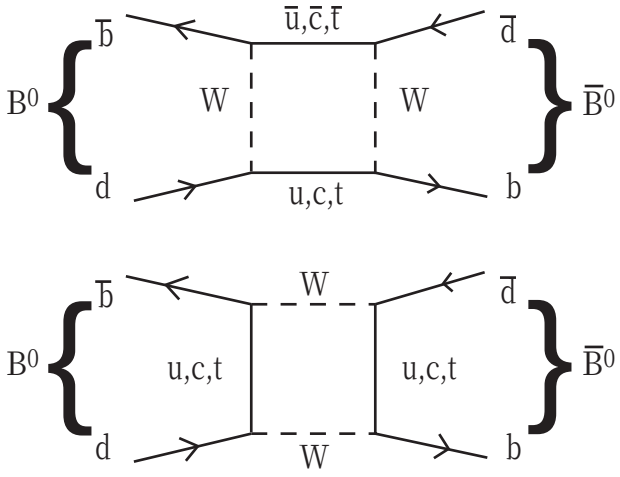

Figure 1.2: Box diagrams responsible for B^0-$\bar{B}^0$ mixing

There are some advantages of producing B mesons at the Υ(4S) energy region. The $B\bar{B}$ cross section is higher than higher center of mass energy. $B-\bar{B}$ pairs are exclusively produced (50% $B^0\bar{B}^0$ and 50% B^+B^-). The energy of the produced B meson is known, which can be used to reduce the combinatorial background.

One of the most promising methods to measure CP angles in B meson system is based on neutral B decays to CP eigenstates f_{CP} which are common to B^0 and $\bar{B}^0$. B^0 and $\bar{B}^0$ can "mix" through the loop diagrams shown as Fig. 1.2. *i.e.* after a certain time, a meson which was B^0 at production will not be a pure B^0 state, but a mixed state of B^0 and $\bar{B}^0$. CP violation is induced by B^0-$\bar{B}^0$ mixing through the interference of the two decay amplitudes of B^0 , $A(B^0 \to f_{CP})$ and $A(B^0 \to \bar{B}^0 \to f_{CP})$. In order to detect this CP violation, one must know, or *tag* the nature of the particle(B or $\bar{B}^0$) at a given time.

On the Υ(4S), tagging one B as a B^0 or a $\bar{B}^0$ identifies the other with certainty. Since both C and P eigenvalue of Υ(4S) is -1 and the decay of Υ(4S) is caused by strong interaction which conserves CP, produced B-$\bar{B}$ should be in a CP eigenstate with eigenvalue of 1. Because spin of Υ(4S) is 1 and that of B is 0, B^0 and $\bar{B}^0$ mesons are produced with the orbital angular momentum of 1, which means the P eigenvalue of B-$\bar{B}$ system is -1. This restricts the C eigenvalue to be -1 and a $B\bar{B}$ pair will remain in a coherent $B\bar{B}$ state as long as neither B has decayed. If one of them is detected to be $B^0(\bar{B}^0)$ at a moment, the other is inevitably $\bar{B}^0(B)$ at that time. This is extremely important for measuring CP violation.

For example, consider one B^0 from Υ(4S) decays into semi-leptonic mode, like $B \to D^* l\nu$ (l = e or μ), after t_1 from its production. If that particle was $B^0(=\bar{b}d)$ at t_1, the charge of lepton is positive (see Fig. 1.3) and if it was $\bar{B}^0(=b\bar{d})$, the charge of lepton is negative. Thus one can tag the flavor of B mesons by detecting leptons from Bs.

When the B^0-$\bar{B}^0$ pair is produced with odd relative angular momentum, the rate for one of the neutral B mesons to decay as $\bar{B}^0$ at $t = t_1$ and the other (which is B^0 at $t = t_1$) to decay into CP eigenstate, for example $J/\Psi K_S$, at

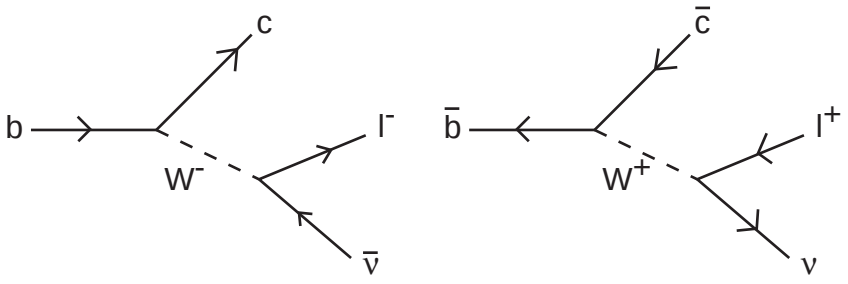

Figure 1.3: Diagrams related to semileptonic B decays. One can identify the flavor of B by the charge of lepton.

$t = t_2$ is written as

$$P[B^0 \to J/\Psi K_S; \Delta t] = \frac{1}{2} e^{-\Gamma|\Delta t|}(1 + \lambda \sin \Delta m \Delta t) \tag{1.9}$$

where Γ is the B meson total decay width, $\Delta t \equiv t_2 - t_1$, Δm is the mass difference between the two neutral B weak eigenstates and λ is the CP violation parameter

$$\lambda = -\sin(2\beta). \tag{1.10}$$

The CP conjugate of this function is

$$P[\bar{B}^0 \to J/\Psi K_S; \Delta t] = \frac{1}{2} e^{-\Gamma|\Delta t|}(1 - \lambda \sin \Delta m \Delta t). \tag{1.11}$$

The Δt values range is from $-\infty$ to $+\infty$ and it is easily seen that CP asymmetry vanishes in the time integrated rate. Therefore, the measurement of decay time difference, Δt is required to observe CP asymmetry in experiments at the Υ(4S).

In the normal colliders with symmetric energy, the Υ(4S) is produced at rest, consequently the B mesons are produced almost at rest. Momenta of Bs from Υ(4S) are about 325 MeV/c and the average decay length of the Bs is about 30 μm, if the Υ(4S) is produced at rest. Any time dependence measurement is impossible with the present vertex detectors for such a case.

A solution is to produce the Υ(4S) moving in the laboratory frame. This can be achieved by colliding two beams of unequal energy. This results in two B mesons boosted in the same direction along the beam axis. The average distance between the two B decays is approximately $\beta\gamma c\tau$ where β and γ are the boost parameters of the center of mass and τ is the average B lifetime. Since the B mesons move almost parallel to the beam axis, the decay time difference of two B mesons can be approximately calculated as

$$\Delta t \simeq \Delta z / \beta\gamma c \tag{1.12}$$

where Δz is the distance of the decay vertices along the beam axis. A precise measurement of the decay vertices of B mesons is necessary to measure CP violation in this scheme.

1.4 KEK-B Factory

The KEK-B Factory is a collider experiment which primary goal is to study CP violation in B meson system.

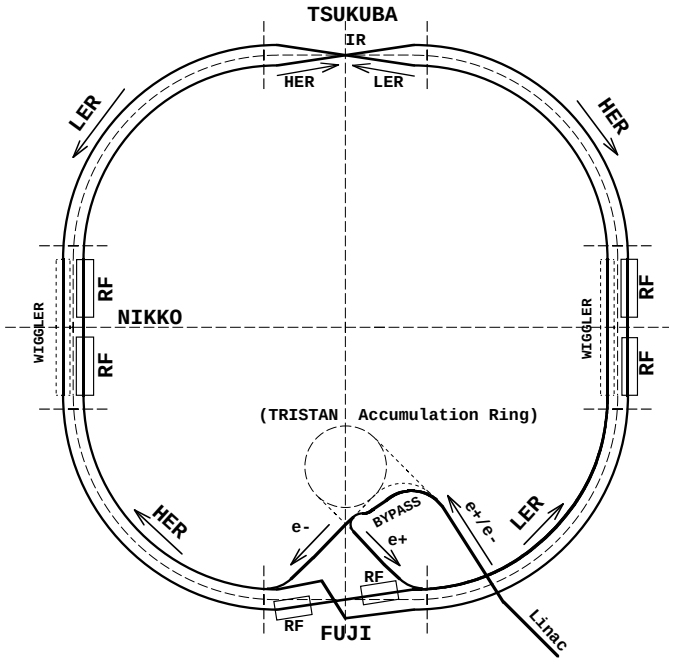

Figure 1.4: The KEKB accelerator

1.4.1 KEKB Accelerator

As described in previous section, to measure CP asymmetry in decays of B mesons, one must produce $\Upsilon(4S)$ boosted in the laboratory frame. KEKB accelerator was designed to realize this. It has two rings in a tunnel which was used for TRISTAN, one for electron beam and the other for positron beam. The circumference of main rings are about 3 km.

Beam energies are chosen to be 8 GeV/c^2 for electron and 3.5 GeV/c^2 for positron, so that center of mass energy comes on $\Upsilon(4S)$ resonance. In such configuration, $\beta\gamma \simeq 0.425$ and the average decay length of Bs from $\Upsilon(4S)$ is about 200 μm in the laboratory frame. (Fig. 1.5)

In order to produce as much B mesons as possible, KEKB accelerator is designed to run at the highest luminosity in the world, $10^{34} cm^{-2} s^{-1}$, corresponding to 10^8 of $\Upsilon(4S)$ in a year.

1.4.2 The BELLE Detector

The BELLE detector (Fig 1.6) is a 4π detector designed for the study of CP violation in B decays[3]. The BELLE detector consists of Central Drift Chamber(CDC), Aerogel Cherencov Counter(ACC) and Time of Flight counter(TOF), CsI calorimeter(ECL), K_L/Muon detector(KLM), and Silicon Vertex Detector(SVD).

As is described in the previous section, precise vertex measurement and flavor tagging of B are required for the study of CP violation.

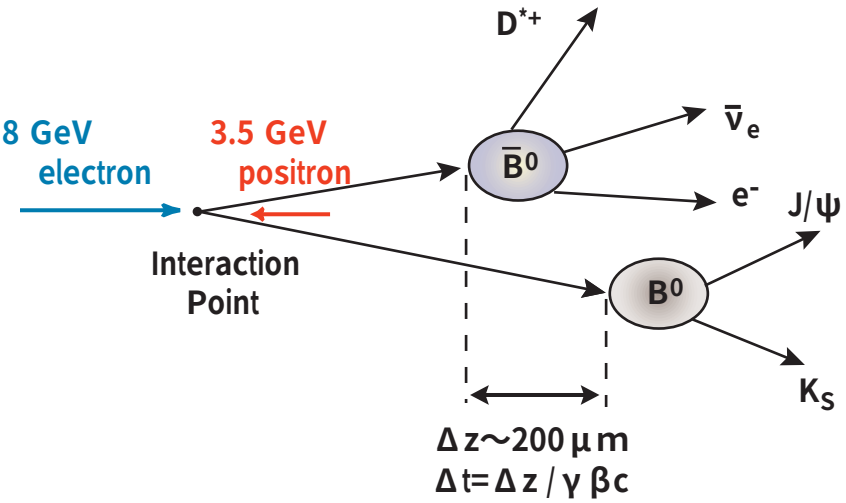

Figure 1.5: A schematic drawing of $B\bar{B}$ decays. The decay time difference is obtained through their decay vertex distance.

There are a number of candidates for vertex detector, *e.g.* scintilating fiber, gas microstrip detector, etc. We decided to use double-sided silicon microstrip detector as vertex detector in the BELLE experiment[4].

The intrinsic resolution order of 10 μm can be achieved by the silicon strip detector. The effect of multiple scattering, which is of great importance in the BELLE momentum region (typically p ~1 GeV), is minimized by use of double-sided silicon strip detector.

The flavor of B meson which decays into CP eigenstate (B_{CP}) is determined by the flavor of the other B meson (B_{tag}). There are mainly two methods to tag the flavor of B. One method is based on semileptonic B decays. The charge of leptons (e and μ) indicates the flavor of the B. The charge of kaon also indicates the flavor of the B, since b $\rightarrow$ c $\rightarrow$ s decay chain is dominant process. Good K/π separation is required for the kaon tagging. The lepton tagging provides clean signals with reasonable efficiency, while the kaon tagging provides high efficiency with large background due to $D \rightarrow K\bar{K}X$ decays.

In the BELLE, electrons are identified by the CDC and ECL. Muons are detected by the KLM. The CDC, TOF and ACC provide K/π separations up to 3.5 GeV/c. The CDC covers the momentum up to 0.7 GeV/c, the TOF covers up to 1.2 GeV/c and the ACC covers the momentum range $1.2 < p < 3.5$ GeV/c.

Charged tracks are primarily reconstructed by the CDC. Photons are detected by the ECL. K_L is detected by the KLM.

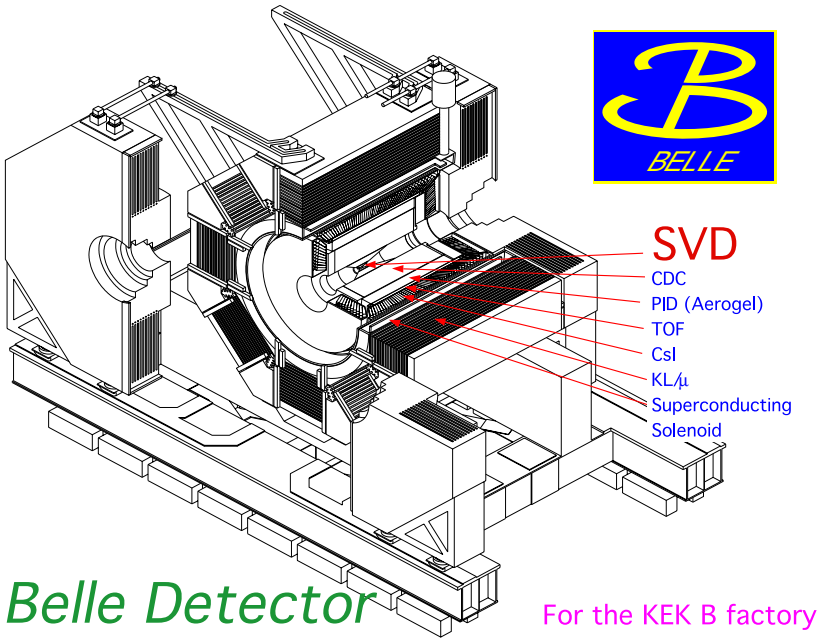

Figure 1.6: The BELLE Detector

Chapter 2

The BELLE SVD

2.1 Requirements for the BELLE SVD

2.1.1 Vertex Resolution

At KEKB, the decay distance of $B\bar{B}$ pairs will be about 200 μm in average. As described in Section 1.3, the projection of the decay distance along the beam direction (Δz) is converted to proper time difference Δt by $\Delta t \simeq \Delta z / c\beta\gamma$, where $\beta\gamma$ is Lorentz boost factor (=0.425 for the KEKB). The measured Δt is smeared by errors in the Δz measurement.

Studies are made for the effects of the finite Δt resolution on the asymmetry measurement and the sensitivity to CP violation. According to it, about 70% more luminosity is needed to establish an effect if the resolution on $\Delta t/\tau_B$ degradates from 0.5 to 1.0.

Based on this result, the target of SVD vertex resolution was set to $< 100\mu$m, half of the average decay distance of $B\bar{B}$ pairs.

The vertex resolution is dominated by two contributions, geometrical factor and multiple scattering effect. In the two layer detector system, impact parameter resolution can be expressed as follows.

$$\sigma_v^2 = \sigma_{geom}^2 + \sigma_{ms}^2 \tag{2.1}$$

$$\sigma_{geom}^2 = \left(\frac{R_1\sigma_2}{R_2 - R_1}\right)^2 + \left(\frac{R_2\sigma_1}{R_2 - R_1}\right)^2$$

$$\sigma_{ms}^2 = \sum_{i=1}^{nscat} (R_i \Delta\theta_i)^2$$

$$\Delta\theta_i \simeq \frac{0.0136}{p[GeV/c]} \sqrt{\frac{x}{X_0}} \left[1 + 0.038 \ln \frac{x}{X_0}\right]$$

where R_1 and R_2 are radii of the layer 1 and 2, σ_1 and σ_2 are intrinsic resolutions.

The first term of 2.1 represents the intrinsic resolution of the detector and the detector geometry. The second term accounts for the effect of multiple scattering in the first detector layer plus any other material before the first measurement. Considering these contributions to vertex resolution, the following three conclusions are drawn:

1. The first measurement (r_1) should be performed as close to the interaction point as possible.

2. The lever arm ($r_2 - r_1$) should be as large as possible.

3. The material of the detector itself, and especially the material in front of the first measurement should be minimized. The average scattering angle of 1 GeV/c particle caused by 300 μm silicon wafer is about 0.6 mrad.

In the SVD, z-resolution is more important to measure CP violation effect. In z-direction, effective thickness of DSSD can be much larger than 300 μm due to possible large incidence angle. For this reason, the final z-resolution is limited by the amount of multiple scattering.

2.1.2 Radiation Hardness

To produce as many B mesons as possible, KEKB accelerator is designed to run at remarkably high luminosity, $10^{34} cm^{-2} s^{-1}$. From its nature, SVD must be placed very near the interaction point and would be subject to great amount of beam background, mainly spent electrons. Fig. 2.1 shows expected radiation dose rate in BELLE environment at SVD position. In this calculation, designed beam currents (2.6 A for positron and 1.1 A for electron) and the vacuum in the beam pipe 10^{-9} Torr are assumed. Reflecting the flat aperture of the beam profile, the background shows ϕ dependency and will be maximum on horizontal plane, ϕ=0. The maximum radiation rate will be about 30 krad/year while the average rate is estimated to be less than 10 krad/year.

In such a high radiation environment, semiconductor devices will be damaged resulting in increase of noise and loss of its functionality. The SVD must survive under such radiation environment at least for several years.

2.2 Detector Configuration

2.2.1 Overview

Taking the detector efficiency into account, at least three layers of sensors are needed to obtain vertex information. The distance between the first layer and interaction point (IP) should be as short as possible, as described in 2.1.1. However, the radiation background grows as getting closer to IP, inversely proportional to the distance from IP. The layout of first layer is decided by the radiation torelance of the electronics we can use and the vertex resolution we need. The distance of the last layer from IP is limited by the radius of the outer detector, CDC. We chose three layer configuration as described later.. The amount of matter used in the mechanical support structure of the SVD is minimized to avoid the effect of multiple scattering, while maintaining good structural integrity.

2.2.2 DSSD

We use double-sided silicon microstrip detector (DSSD) as vertex detector. For the principle of silicon strip detector, see Appendix A.

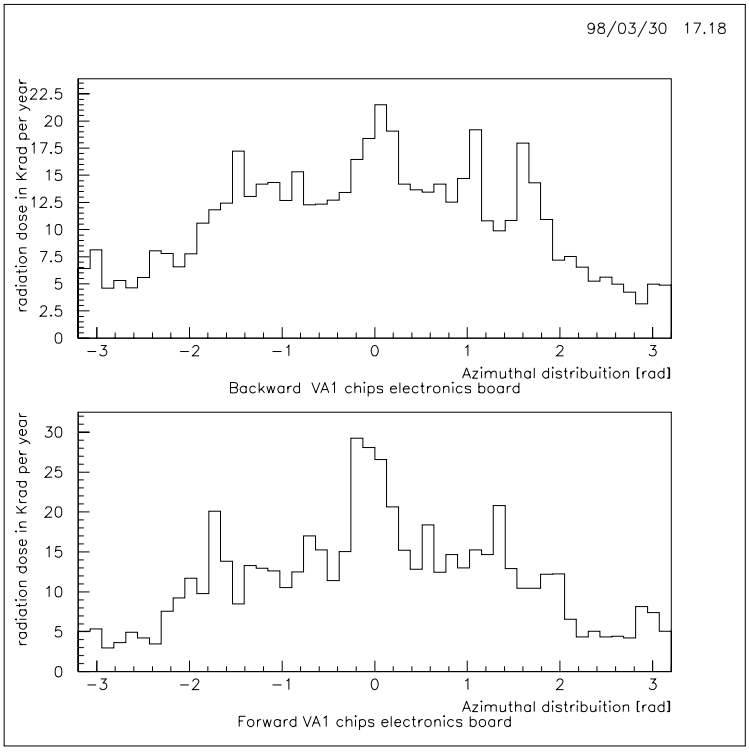

Figure 2.1: Expected radiation dose per year as a function of azuminal angle

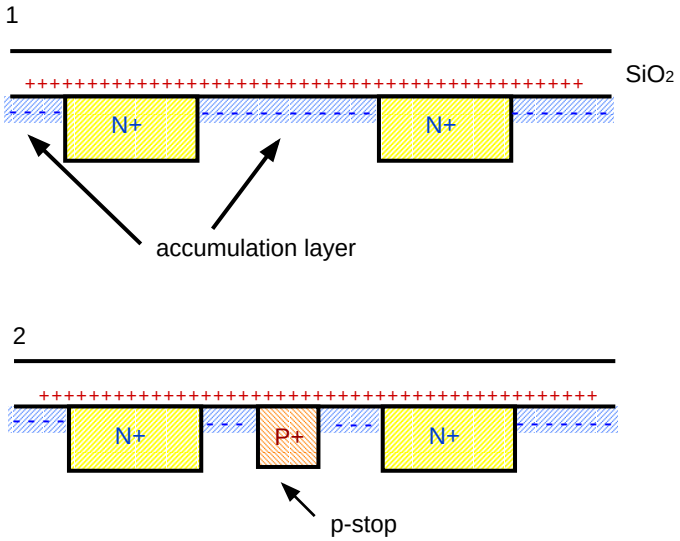

Figure 2.2: A schematic drawing of p-stop

We chose a DSSD, S6936, on a Hamamatsu Photonics Catalogue. This DSSD is originally designed for DELPHI experiment at CERN. Table 2.1 shows BELLE specifications for S6936.

In a DSSD, p^+ and n^+ strips are formed on both side of substrate, perpendicular to each other. When both sides are used for readout, a problem arises on the surface where the ohmic contact will be obtained (n^+ strips in the case of n^- substrate). As is well known, the oxide layer formed during the passivation of the crystal, before n^+ implantation, becomes a site of fixed positive charges. Therefore negatively charged layer is formed in the interface region and allows an interstrip conductivity between the n^+ strips (figure 2.2 1). To avoid this, p^+ strips are implanted between n+ strips (figure 2.2 2), which isolate strips. These p^+ regions are called as p-stop.

An S6936 DSSD has 1280 sense strips and 640 readout pads on each side. All sense strips are biased via 25 MΩ polysilicon bias registers. The detector employs integrated AC coupling capacitors on both sides to capacitive signal readout from floating strips.

Ohmic (n-) side is chosen to be the z-side. In order to readout the signal of z-strips along the beam axis, an additional layer is formed on top of and orthogonal to the z sensitive strips. This structure is called as double metal layer (DML) structure. The z-strip pitch is 42 μm and adjacent strips are connected to one readout trace on the second metal layer. The ϕ(p)-strip pitch is 25μ and every other strips are connected to the readout pads.

The detector capacitance per one readout strip is measured to be 7 pF for p-side and 22 pF for n-side, respectively. The capacitance of n-strip is much larger than that of p-strip since two adjacent strips are connected to one trace and the DML structure are employed.

The intrinsic resolution depends on the position calculation algorithm. If one simply takes the center of clusters as the hit position, the resolution would be $1/\sqrt{12}$ of the readout pitch, about 14 μm for p-side and 24 μm for n-side,

for normal incident tracks.

Table 2.1: BELLE specifications for S6936

Parameter	p-side	n-side
Chip size	57.5mm×33.5mm	
Active Area	54.5mm×32.025mm	53.76mm×32.04mm
Thickness	$300 \pm 15\mu$m	
Readout(Bias) method	AC(Poly-Si)	AC(Poly-Si)
Strip pitch	25μm	42μm
Number of strips	1281	1280
Number of readout strips	641	640
Strip width	8μm	8μm
Readout electrode width	8μm	14μm
DML insulator material, thickness	N/A	SiO_2, 5μm
DML trace pitch, width	N/A	48μm, 8μm
Full depletion voltage (Vfd)	80V Max	
Breakdown voltage	100V Min	
Leakage current at Vfd	2μA Max	
Bias resistance	25MΩ Min	25MΩ Min
Coupling capacitance at 10kHz	55pF	40pF
Breakdown voltage of coupling capacitor	30V Min	100V Min
Load capacitance at 1MHz	8pF	20pF
Number of NG channel	19 Max	19 Max
Passivation	SiO_2	SiO_2

2.2.3 Detector Layout

Definitive configuration of BELLE SVD is presented in Fig. 2.3. SVD consists of three cylindrical layers of DSSDs. Inner, middle and outer layer consists of eight, ten and fourteen detector units, called as "ladders", respectively. This configuration covers a polar angle of 21° to 140° in the laboratory frame, corresponding to an angular acceptance of 0.86 in the center of mass frame of $\Upsilon(4S)$. The radial distances from interaction point to the inner, middle and outer layer are 30mm, 45.5mm and 60.5mm, respectively.

2.2.4 Mechanical Structure

The SVD consists of thirty two ladders, end rings, support cylinders and some covers as shown in Fig.2.4.

Each ladder is made of two half-ladders that are mechanically joined by a support structure but electrically independent of each other. Fig.2.5 shows a schematic drawing of ladders for all three layers. To reduce the types of fixtures and parts necessary for ladder assembly, the ladder is designed as symmetrical as possible. As a result, only two types of half-ladders are necessary: a "short" half-ladder with single DSSD and a "long" one with double DSSDs. Each type of half-ladder consists of DSSD(s), hybrid boards with readout chips and support structure.

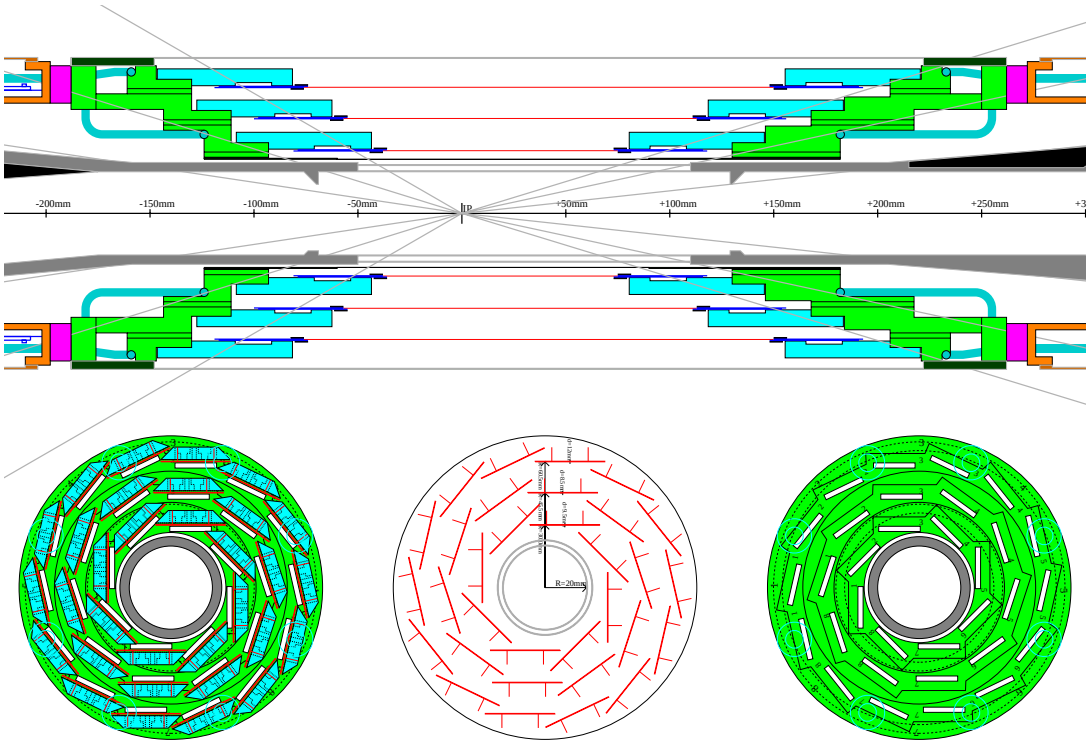

Figure 2.3: The configuration of SVD

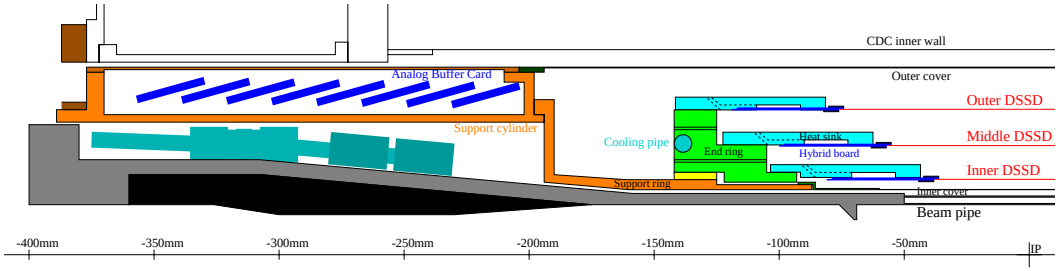

Figure 2.4: Overview of the SVD support structure

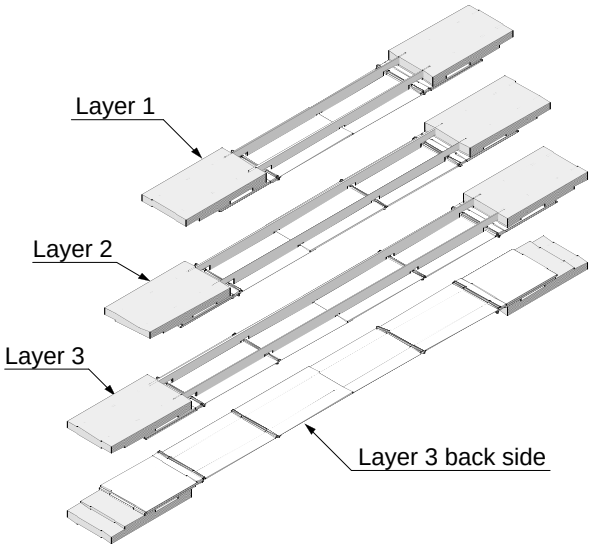

Figure 2.5: A schematic drawing of SVD ladders

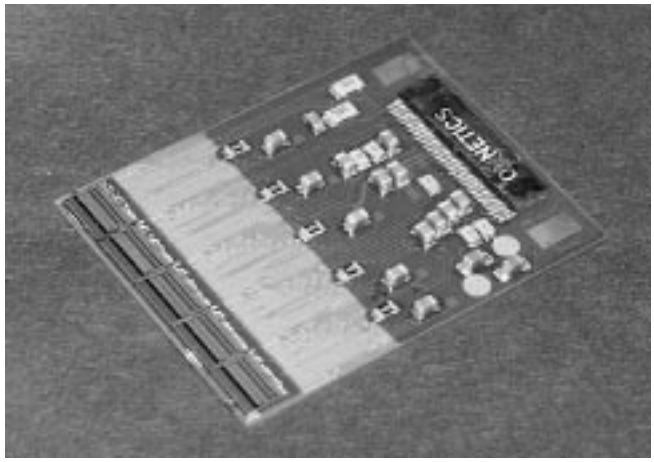

Figure 2.6: A picture of BELLE SVD hybrid board

Figure 2.7: A schematic view of hybrid unit

Ladders are mounted on the forward and backward end rings which are attached to the forward and backward support cylinders. The support cylinders are supported by the CDC(Central Drift Chamber) end plates.

Detector Unit

A detector unit consists of either a single detector or two detectors with an overlapping joint. In order to minimize the noise of the double-detector module, different sides of the two detectors were connected. *i.e.* p-side of one detector was connected to n-side of another.

Hybrid Unit

A hybrid unit consists of two single-sided hybrid boards glued back-to-back. Five VA1 readout chips are mounted on each hybrid board. (Fig. 2.6) The circuitry is printed on a multilayer aluminum nitride substrate produced by the Kyocera company in Japan.

Fig. 2.7 shows a schematic drawing for a hybrid unit. Since the preamplifier chips are heat source, careful attention was paid to the thermal path way through the hybrid, across glue joints, and into heatsink. Hybrid boards were made of aluminum nitride, whose heat conductivity is expected to be high (150-200 W/mK). To increase heat conductivity, a boron nitride loaded epoxy, whose thermal conductivity is expected to be about 1 W/mK, was used to join the two hybrids.

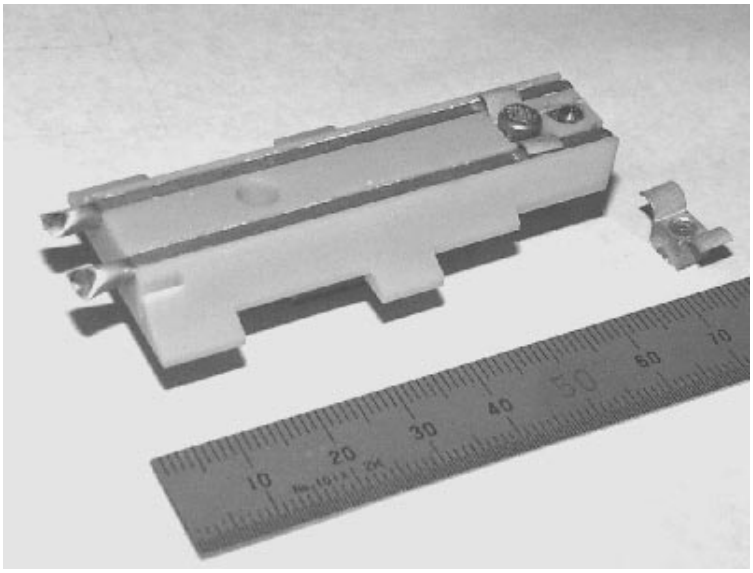

Figure 2.8: A picture of heatsink with heatpipes embedded

Heatsink

The heatsink was made of aluminum nitride, whose high thermal conductivity (150-200 W/mK) and low coefficient of thermal expansion (2-3 ppm/K) made it an attractive option for both heat conduction and mechanical support. The thermal conductivity was enhanced by embedding two heatpipes in the heatsink. Measurements indicate that the total temperature drop across the heatsink will be 1.8°C at normal preamplifier power levels. Fig.2.8 shows a picture of the heatsink.

Support Structure

In order to support the ladder mechanically, boron nitride ribs reinforced by CFRP sheets were used. Two boron nitride ribs were glued to heatsinks and DSSDs using epoxy. Total amount of material is less than $0.1\% X_0$ per layer.

2.3 Readout Electronics

2.3.1 Overview

The signals from DSSD are read out by VA1 chip mounted on hybrid board and transferred via thin cables to a buffer card (ABC) followed by thicker cables and a repeater board (REBO). The REBO drives a $\sim$ 30 m long cable to send differential output to the receivers located in the electronics hut, where Flash ADC (FADC) cards are installed to digitize the analog signal and send the digitized signal to the central DAQ system.

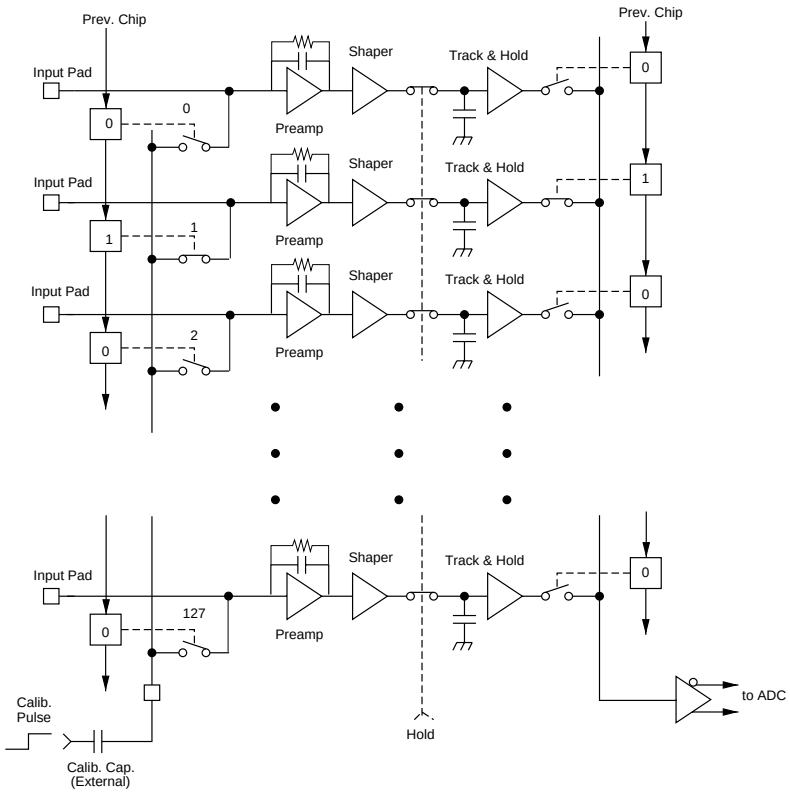

Figure 2.9: Block diagram of VA1 chip

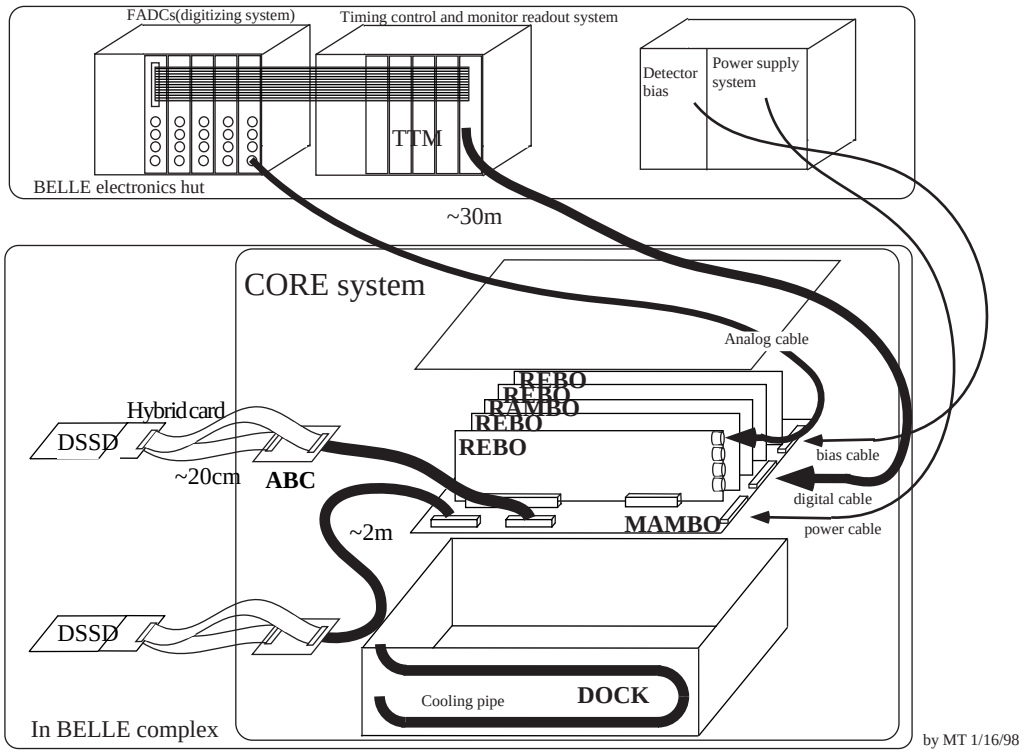

Figure 2.10: Repeater system for BELLE SVD

2.3.2 VA1 Chip

VA1 chip, which is originally developed at CERN and commercially available from IDEAS, Oslo, Norway, is used as frontend VLSI chip. The VA1 is 128 channel CMOS integrated circuit designed for the readout of silicon vertex detectors and other small signal devices. It has extremely good noise performance (equivalent noise charge = 165 e^-+6.1e^-/pF with 2.5 μsec shaping time) and consumes only 1.2 mW/channel.

Fig. 2.9 shows the block diagram of the VA1 chip. Signals from the strips are amplified by a charge sensitive amplifier, followed by a CR-RC shaper and sample and hold circuit. The output voltage is read out sequentially when trigger comes. A single bit propagating through a shift register causes the output switches to output amplifier to be closed one at a time. In this way, all 128 channels in a chip can be read out through a single ADC.

2.3.3 CORE (COntrol and REpeater) System

Repeater system consists of small cards near the detector (ABCs), boards for signal buffering and frontend control (REBO), a board for monitoring (RAMBO), a mother board (MAMBO) and their cooling and shielding case (DOCK).

Signals from a side of DSSD are read by five VA chips on a hybrid board and sent to repeater system through special 30 wires thin cables, which were provided by Omnetix Co. ltd, USA. Two cables from two hybrid boards are

merged on a small printed circuit board (ABC) with 50 wires flat cable. The flat cable is connected to a mother board (MAMBO) contained in a small crate (DOCK). A MAMBO has five slots. A printed circuit board for monitoring purpose (RAMBO) occupies the center slot, and four frontend readout and control boards (REBOs) use the other slots.

Signals from ABC are sent to REBO through a local bus. After amplification and filtering, differential signals are sent to backend electronics system located in the electronics hut. A thermistor is mounted on each hybrid board to monitor the temperature of the frontend electronics. Voltage on a thermistor is read out by RAMBO. All the timing and control signals, bias voltages and power supplies from backward electronics are fed to MAMBO and then distributed to each board or sent to frontend electronics.

Since DOCK can control and read out eight ABCs (or 16 hybrids), we needed 8 DOCKs (8 MAMBOs and RAMBOs, 32 REBOs) for 128 hybrids on 32 ladders.

2.3.4 Expected Noise Performance

The noise of the SVD has following components.

1. Noise in the VA1 preamplifier chip. Noise performance of VA1 chip with 2.5μsec shaping time is

$$ENC_{VA} = 165 + 6.1C_d$$

   where C_d is the total detector capacitance seen by the VA1 chip.

2. Noise from detector leakage current. Equivalent noise charge of this component is calculated as

$$ENC_{lc}^2 = \frac{1}{2\pi}\int_0^\infty 2qI_{leak}|H(\omega)|^2 d\omega$$

   where H(ω) is the response function of the readout chip, q is the electron charge and I_{leak} is the leakage current. For our system,

$$ENC_{lc} \simeq 110\sqrt{I_{leak}T_p}$$

   where the unit of I_{leak} is nA and T_p is shaping time in the unit of μsec.

3. Noise from bias register.

$$ENC_{bias}^2 = \frac{1}{2\pi}\int_0^\infty 4kTR_b|H(\omega)|^2 d\omega$$

   where R_b is bias resistance, k is the Boltzmann constant and T is the absolute temperature. For our system,

$$ENC_{bias} \simeq 800\sqrt{R_bT_p}$$

   where the unit of R_b is MΩ.

4. Excess noise on n-side. The origin of this component is p-stop resistance on n-side. ENC_{ex} is measured to be $\sim 600e^-$ [5].

Table 2.2: Expected noise and S/N before irradiation. Signal is assumed to be 16500 e^-.

side	ENC(e^-)	S/N
p	487	34
n	802	21
p+n	930	18

Table 2.3: Detector parameters assumed in the noise estimation

item	value
load capacitance	7 pF for p-side and 22 pf for n-side
leakage current	2.1 nA per channel
bias resistance	25 MΩ
excess noise on n-side	600 e^- per channel

The total noise of SVD is calculated as

$$ENC_{total} = \sqrt{{ENC_{VA}}^2 + {ENC_{lc}}^2 + {ENC_{bias}}^2 + {ENC_{ex}}^2}.$$

The expected noise level and S/N ratio for the SVD is summarized in Table 2.2. The detector parameters relevant for this estimation are listed up in Table 2.3.

Chapter 3

Ladder Assembly

Ladder assembly was performed in following way.

1. Gluing detectors and hybrids to form half-ladders
2. Wire bonding (detector-detector and detector-VA1 chip)
3. Burn-in to find potential punch-through in coupling capacitors
4. Gluing two half-ladders, heatsinks and support ribs to form full-ladders

3.1 Gluing Two Detectors

To produce a double-detector module, two detectors were glued using an alignment fixture.

To glue two detectors, we used the same epoxy as UCSB people used in CLEO experiment, chiba-AW106. Glue had to be applied to a detector in a controlled manner. A machine controlled syringe was used to regulate the amount of glue applied. The amount of glue and time from mixing before use was studied and optimized using dummy detectors. After glue was applied to a detector, the detector was placed on the top half of alignment fixture.

The alignment fixture consists of an aluminum pedestal, a Teflon bed, vacuum chucks and Teflon alignment pins. For alignment, a detector was placed on the Teflon bed and slid up against the alignment pins as shown in Fig 3.1(1). All the material which contact the detector should be soft to avoid scratching or cracking the detector. The sliding bed was made of Teflon to reduce the possibility of wearing passivation layer. The alignment pins were also made of Teflon because hard pin could chip the edge of a detector. The accuracy of alignment in the XY direction was determined by the accuracy of the Teflon pin machining (20μm) and detector dicing(5-10μm).

After the detector was aligned, it was held by vacuum. The other detector was aligned and held in the same way to the bottom half of fixture.

In order to control the final precision of the DSSDs for gluing, the bottom fixture has two alignment pins and the top fixture has two alignment holes. After two DSSDs were attached to the fixtures, the top fixture was brought down to the bottom fixture, guided by alignment pins and holes (Fig 3.1(2-3), Fig. 3.2). The height of spacers between the two fixtures determined the final

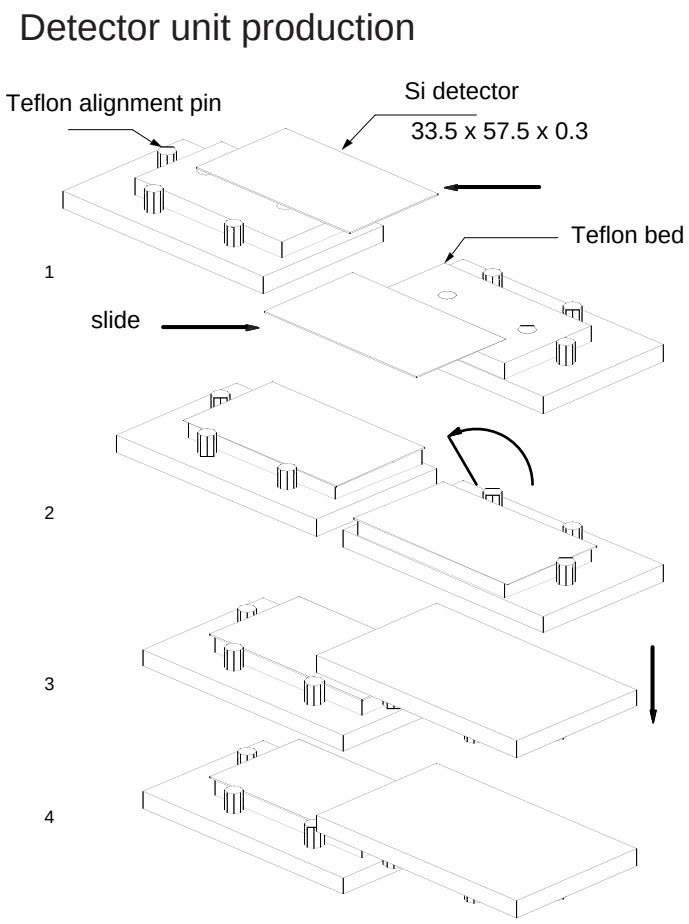

Figure 3.1: Detector unit assembly procedure

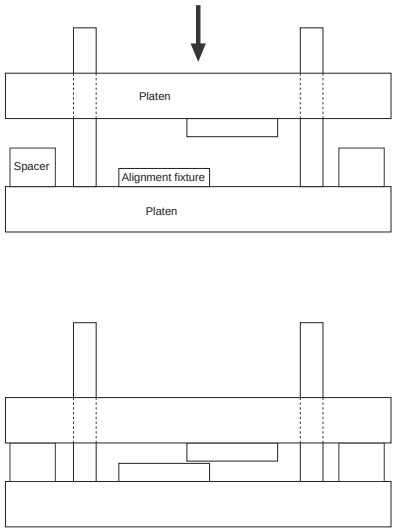

Figure 3.2: Alignment of two DSSDs

position of the detectors, as shown in Fig. 3.2. Finally, fixtures were completely fixed by screws.

DSSDs were held in the fixed position for one day to cure the epoxy. Temperature of the assembly room was controlled to be higher than 25° C in order to guarantee the strength of gluing. Humidity is also controlled to keep the quality of sensor.

3.2 Gluing Two Hybrids

Two single-sided Hybrid boards are glued back-to-back to form a double-sided hybrid module. Boron nitride loaded epoxy was used as glue in order to make path for the heat generated by VA chips.

In order to control the thickness of hybrid unit, the amount of glue was changed according to the thickness of hybrid boards. The designed thickness of hybrid boards was 500 μm while that of the real products varied from 490 μm to 550 μm. The thickness of hybrid boards were measured and the combinations were arranged so that the total thickness of two hybrids are averaged.

According to the size of measured gap between two hybrids, the amount of glue was controlled to fill as much space as possible. The viscosity of glue was sensitive to the temperature.

Two hybrids were glued by similar manner as DSSD-DSSD gluing. Glue was applied to one hybrid board. That hybrid was placed in bottom fixture and aligned(Fig. 3.3 (1-3)). The other hybrid was held on top fixture by vacuum in roughly aligned position. Top and bottom part of fixture were brought together. Hybrids were pressed against alignment pins by an alignment bar and aligned precisely(Fig. 3.3 4). Since there is 1.6 mm of difference between the designed position of two hybrids along the long boundary, the alignment fixture was designed as step with 1.6 mm of width. Hybrid boards were kept in aligned position for one day to cure the glue.

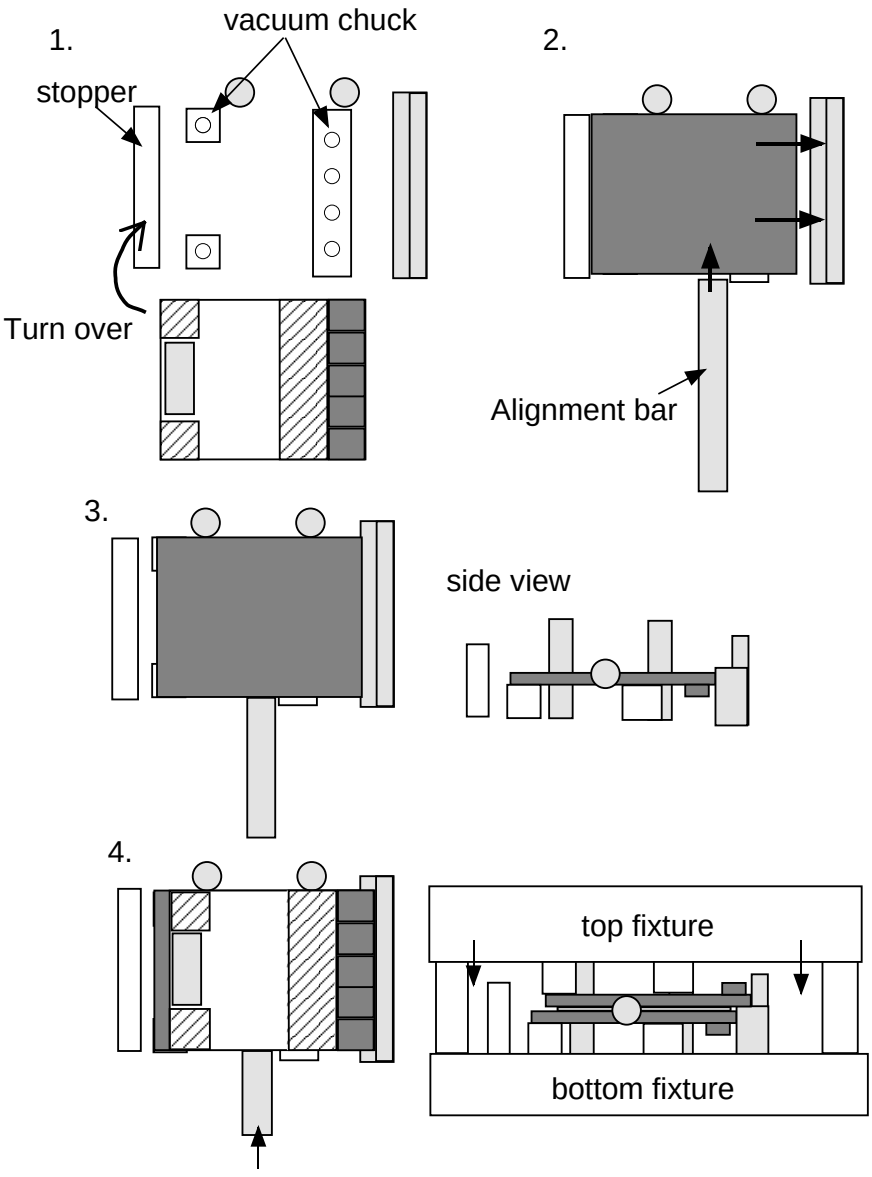

Figure 3.3: Procedure of hybrid unit assembly

3.3 Gluing Detector and Hybrid Unit

A hybrid unit and a single detector(for *short* half ladders) or double-detector unit(for *long* half ladders) were glued together to form a half ladder unit.

The procedure was almost the same as that of detector-detector gluing. The same epoxy as DSSD-DSSD gluing was used and it was applied on an edge of detector unit by dispensing machine. Detector unit was placed on Teflon bed and aligned by alignment pins. Hybrid unit was placed on the other table on the same pedestal and aligned by pins. (Fig. 3.4) It was also fixed in Z direction by a stick. The table for hybrid was able to move vertically and it was moved higher than aligned position when hybrid unit was placed. The hybrid table was brought down to the desired position and fixed by screws.

3.4 Wire Bonding

Once a half ladder was assembled, wire bonding was done between readout chips and detector, and for long half ladders, between detectors.

An automatic wire-bonding machine was used under control of HPK technicians. NG strips are not wire-bonded. Fixtures for holding half ladder during bonding were made so that after binding one side, one could reverse the half ladder to wire the other side.

In the early stage, we suffered from bad bonding pads on readout chips which tend to come off from the surface of chip. The failure rate was 5-10 wires per a side(640 channels), depending on the condition of chip surface. Once bonding machine failed, we had to stop the bonding, remove the failed wire and repeat the wire-bonding using spare pad. This took a certain amount of time and constrain the production rate of ladders to one half ladder per a day. But after some study and configuration, the failure rate dropped to less than three wires per side and production rate increased to two short half ladder or 1.5 long half ladder per a day.

3.5 Test Bench

Electric readout test was performed at each stage of assembly: receiving hybrids, after gluing, after wire-bonding and before full ladder assembly.

The test bench consisted of repeater system, power supplies for repeater system and detector biasing and notebook PC.

Noise and gain performance of each channel was measured to find any problem.

The test bench was also used to find punch-through in AC coupling capacitors of detectors. When new punch-through develops, biasing condition is disturbed around the punch-through and strips in this region become very noisy. Wire-bonding to the punch-through strip must be removed to avoid the effect before full ladder assembly, since it is difficult to repair punch-through with the full-ladder.

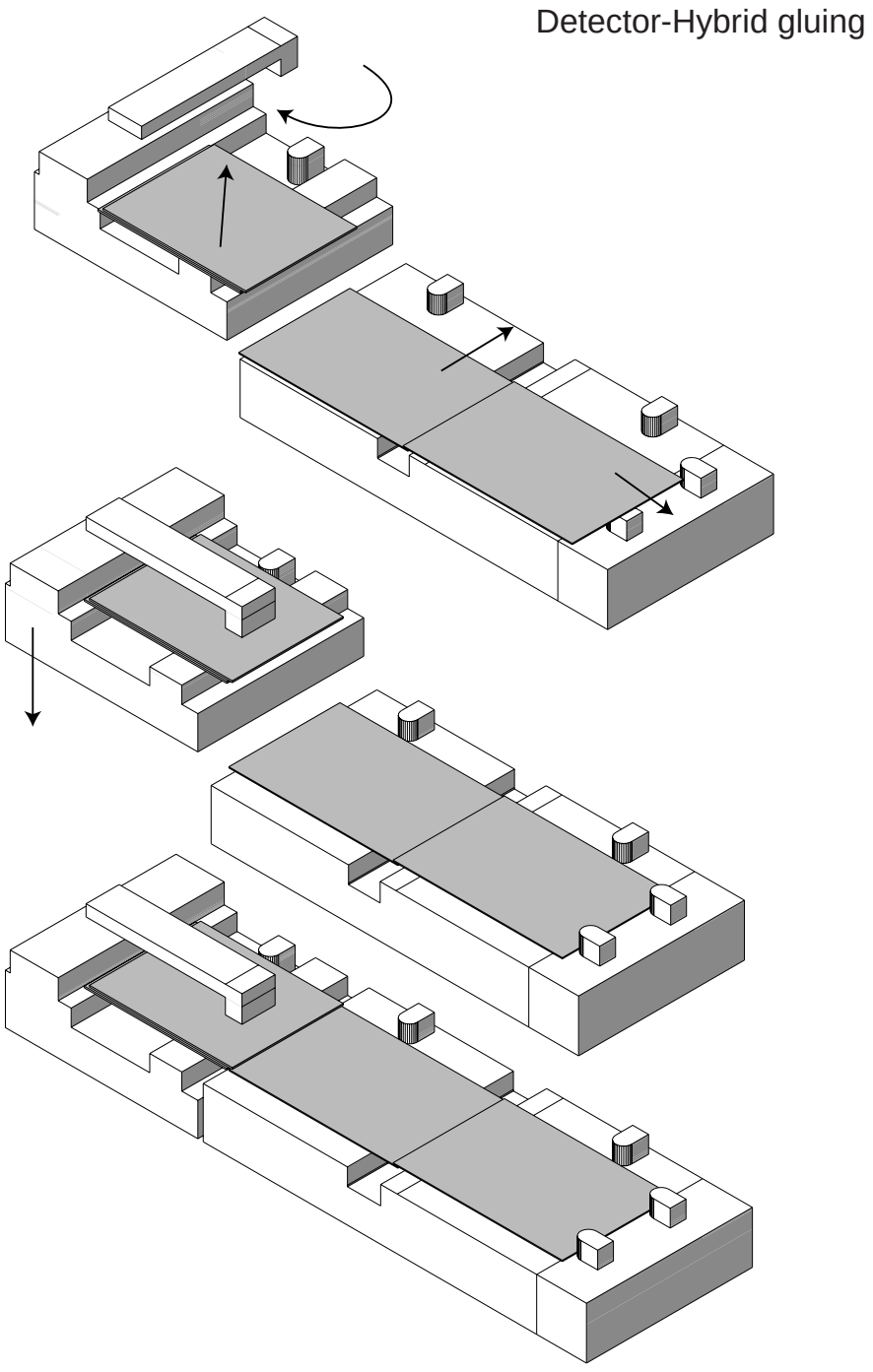

Figure 3.4: Procedure of detector-hybrid assembly

3.6 Burn In

As is mentioned above, punch-through in the coupling capacitors of detectors should be disconnected before full ladder assembly. All the sensors were checked before assembly and punch-through strips were not wire-bonded. However, if there are coupling capacitors not strong enough against biasing voltage, they may be broken and become new punch-through during operation. By applying higher biasing voltage than normal operation (80V for n side and 0V for p side), we tried to find out these potential punch-through strips.

100V(+95V/-5V) bias voltage was applied to each half-ladder for forty eight hours, which corresponds to about ten years of normal operation. A PC controlled the voltage source and monitored the dark current, and automatically shut down the voltage when new punch-through developed and large dark current flowed. Since we found most of punch-through strips at test bench stage before burn-in or in the first few minutes of burn-in process, the stress with power on/off might be the source of new punch-through strips. Therefore, bias voltage was turned off and on twenty times during burn-in. When new punch-through strips developed, corresponding channels were identified from test bench data and wires connecting those channels were removed.

In the early stage, the test of coupling capacitor before assembly process was performed by applying 100V to the n-side of DSSD. However, more punch-through channels than expected were developed during test bench and burn-in process. Most of punch-through were developed in a few minutes after bias voltage was applied. We found most of these channels had been tagged as weak (but not so weak as tagged as bad channel) at the test before assembly. Test voltage was raised from 100V to 120V in order to exclude these channels beforehand. The number of newly developed punch-through channels was decreased from 0.65 channels / DSSD to 0.08 channels / DSSD after raising the test voltage.

3.7 Full Ladder Assembly

After passing burn in process and all the punch-through strips disconnected, half ladders were assembled in pairs to form full ladders.

Half-ladders were paired based on their strip yields to optimize the total detector efficiency. Short half ladders of highest quality (with strip yield better than 98%) were used for the inner layer, since the resolution of the inner layer dominates the impact parameter resolution. The rest of short half ladders and long half ladders with better quality were assigned to the middle layer. The low-quality units were used for the outer layer ladders, since the effect of acceptance loss was minimized.

To build a full ladder, two half ladders were joined using epoxy. The gluing procedure was almost the same as detector-detector gluing. Then, heatsinks were glued onto each end, on the hybrid units using boron nitride loaded epoxy. Finally, support ribs were glued on detectors. Each edge of rib was inserted to the channel of heatsink and fixed by epoxy.

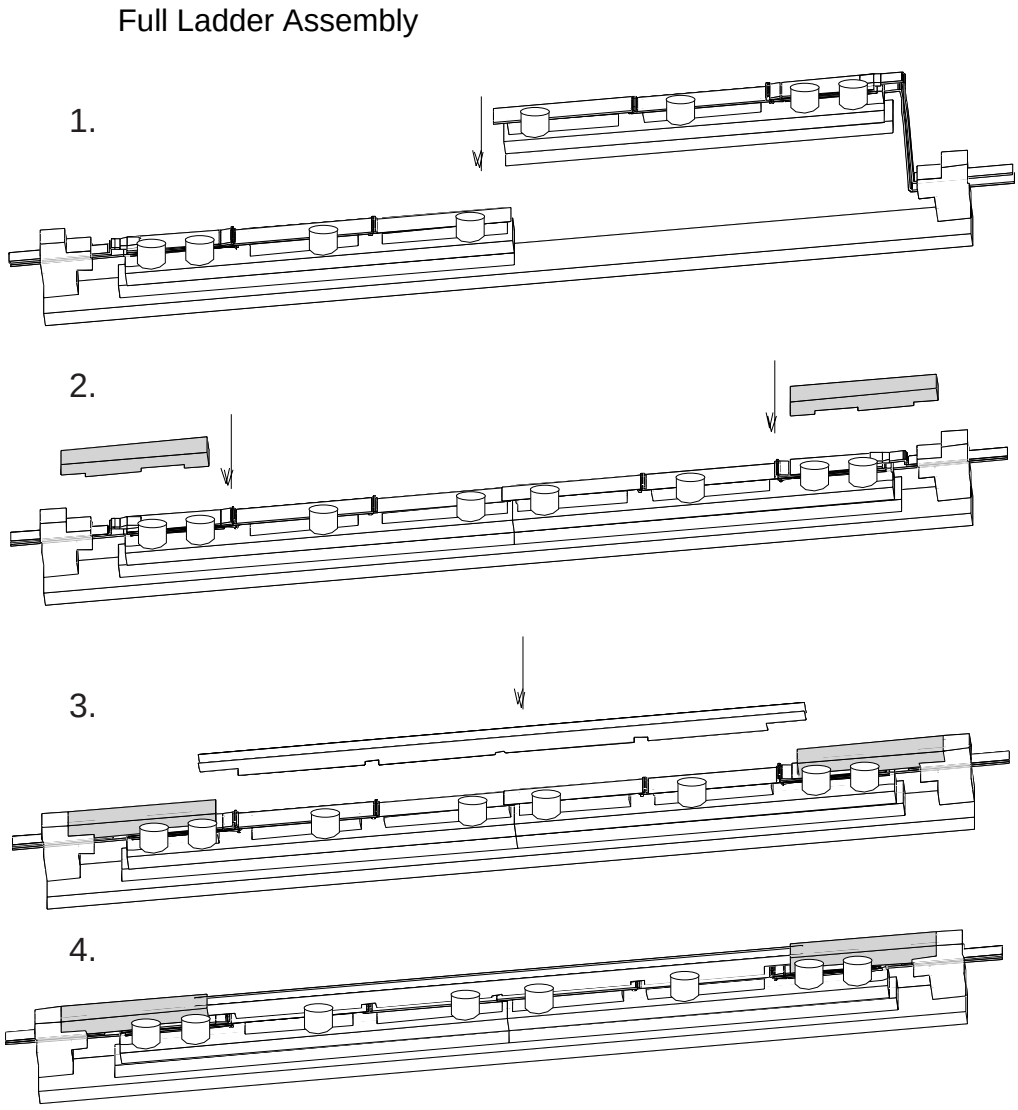

Figure 3.5: Procedure of full ladder assembly

Table 3.1: Strip yields for inner layer

	Test bench		Laser scan	
Ladder#	Forward	Backward	Forward	Backward
0	0.991	0.988	0.986	0.979
1	0.987	0.984	0.989	0.958
2	0.995	0.994	0.993	0.994
3	0.996	0.991	0.995	0.988
4	0.991	0.985	0.990	0.971
5	No data	No data	0.982	0.987
6	No data	No data	0.985	0.983
7	0.996	0.993	0.994	0.991
Average	0.993	0.989	0.989	0.981

Table 3.2: Strip yields for middle layer

	Test bench		Laser scan	
Ladder#	Forward	Backward	Forward	Backward
8	0.940	0.966	0.920	0.948
9	0.982	0.974	0.979	0.965
10	0.964	0.969	0.958	0.968
11	0.974	0.984	0.974	0.972
12	0.982	0.971	0.972	0.942
13	0.964	0.968	0.959	0.961
14	0.961	0.974	0.966	0.934
15	0.966	0.975	0.965	0.971
16	No data	No data	0.973	0.955
17	0.959	0.971	0.956	0.947
Average	0.966	0.972	0.962	0.956

3.8 Laser Scanning Test

After all the assembly, laser scanning test was performed. All the strips were scanned by laser light and signal was read out to measure the relative gain. The relative gain was defined as the ratio of signals from a certain strip on the scanning and signals from the opposite side strip. This complements the gain measurement performed by the test bench in which the gain was measured using test pulse.

Final strip yields are shown in tables 3.1, 3.2 and 3.3. The difference between the strip yields from two measurements might be due to the difference of the definition of bad channel. In the test bench measurement, channels with noise larger than 2000 e and channels not connected to strip were tagged as bad channel. In the laser scanning test, channels with noise larger than 2700 e and channels with no signal observed were tagged as bad channel. In addition, strips with low relative gain were also tagged as bad channel in the laser scanning test.

All the ladders has strip yield better than 90%. Especially, the strip yield of inner layer, which is most important for the vertex measurement, is better than 98% except one ladder.

Table 3.3: Strip yields for outer layer

	Test bench		Laser scan	
Ladder#	Forward	Backward	Forward	Backward
18	0.965	0.946	0.905	0.930
19	0.946	0.956	0.887	0.939
20	0.959	0.971	0.927	0.918
21	0.964	0.961	0.959	0.927
22	No data	No data	0.940	0.961
23	0.959	0.961	0.948	0.959
24	0.966	0.960	0.950	0.931
25	0.953	0.939	0.935	0.918
26	0.967	0.970	0.909	0.960
27	0.970	0.970	0.970	0.938
28	0.967	0.973	0.963	0.972
29	0.972	0.973	0.959	0.961
30	0.953	0.939	0.929	0.950
31	0.932	0.954	0.891	0.945
Average	0.959	0.959	0.934	0.944

Table 3.4: Summary of strip yield for each ladder. Result of laser scanning test is used.

Yield(%)	90-92	92-94	94-96	96-98	98-100	total
Layer 1	0	0	0	1	7	8
Layer 2	0	1	4	5	0	10
Layer 3	3	5	5	1	0	14

Chapter 4

Performance of the SVD

4.1 Expected Vertex Resolution

Figures 4.1 shows expected vertex resolutions obtained by GEANT based Monte Calro simulation. The difference between generated and reconstructed values for tagging side B (B_{tag}) and CP side B (B_{CP}) vertices (V_{tag}, V_{CP}) and their distance (V_{dif}) were plotted and fitted by double-gaussian. The resolution was calculated in weighted r.m.s. method,

$$\sigma = \sqrt{{s_n}^2 f + {s_w}^2 (1-f)}$$

$$f = \frac{h_n s_n}{h_n s_n + h_w s_w}$$

where $s_n(s_w)$ and $h_n(h_w)$ are sigma and height of narrow (wide) gaussian, respectively. Calculated vertex resolutions were $48 \pm 0.5, 83.7 \pm 1.8$ and 98.6 ± 2.3 μm for V_{tag}, V_{CP} and V_{dif}, respectively.

It satisfies the requirement, $V_{dif} < 100$ μm.

4.2 Radiation Hardness

Radiation hardness of the DSSD and the VA1 chip were measured using samples from the same batch as DSSDs and VA1 chips we used.[6][7] DSSD sensors and VA chips were separately irradiated by γ-ray from ^{60}Co source. The average dose rate was about 1 krad/min and total radiation dose was 200 krad for both sensors and VA chips.

4.2.1 DSSD

When silicon strips are exposed to radiation, the bias leakage current increases. Since increase of leakage current degradates the noise performance of detector, we studied the radiation tolerance of our DSSD. Fig. 4.2 shows the increase of the leakage current of a DSSD as a function of the total radiation dose. The DSSD was biased during irradiation. Leakage current increased linearly with the radiation dose. The damage constant was 4.2 nA/krad/cm^2, which is consistent with the reported value of CLEO SVX detector, 5 ± 1 nA/krad/cm^2[8].

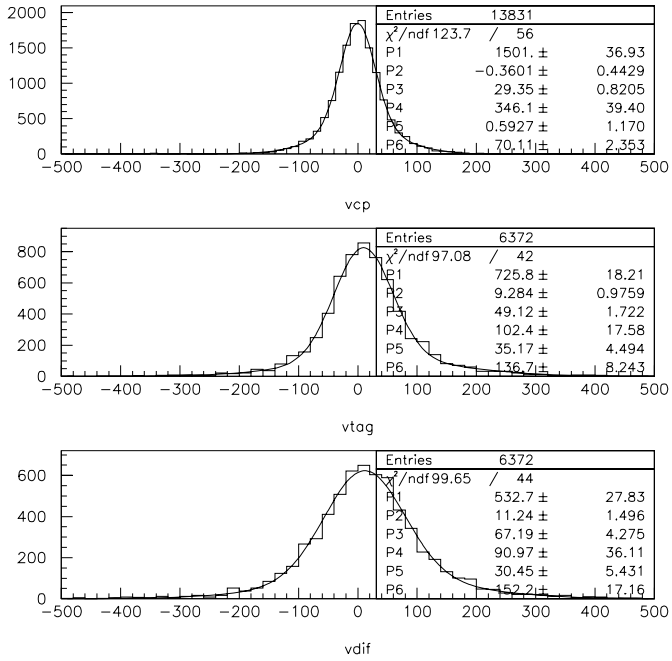

Figure 4.1: Vertex resolutions for $B_{tag}(V_{tag})$, $B_{CP}(V_{CP})$ and difference of two Bs (V_{dif}). The unit of horizontal axes are μm.

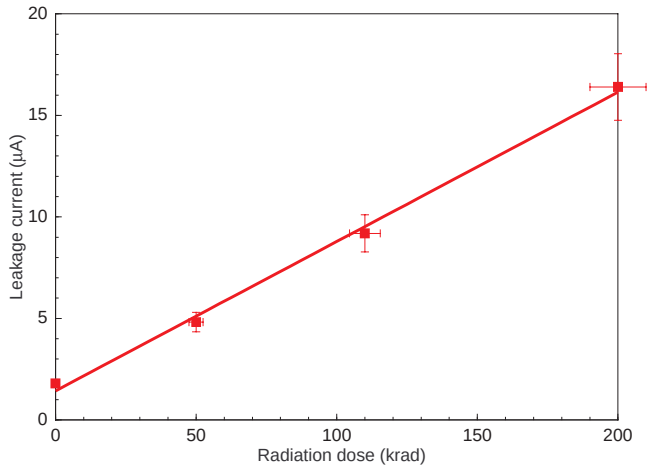

Figure 4.2: DSSD leakage current as a function of radiation dose

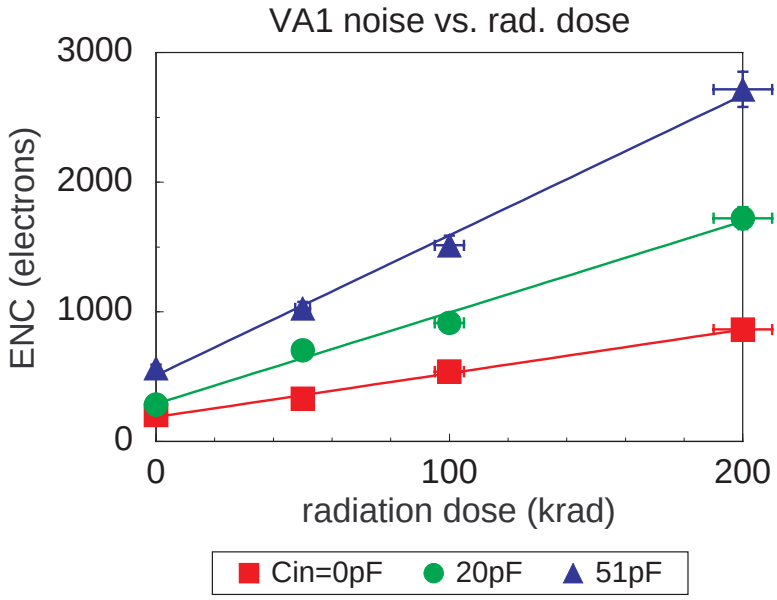

Figure 4.3: Noise performance of VA1 chip as a function of radiation dose

4.2.2 VA1 chip

In order to simulate the running environment in the BELLE, the VA1 chip was supplied with proper DC bias voltages and currents during irradiation. Measurements were performed with the accumulated radiation dose of 0 krad, 50 krad, 100 krad, 200 krad. In each measurement, values of bias currents and voltages were adjusted to hold proper shaping time(1.7 μsec) [1] and to minimize amplifier noise. The equivalent noise charge (ENC) was deduced from r.m.s. value of the pedestal fluctuations observed in 10^3 readout cycles and the measured amplifier gain.

Fig. 4.3 shows equivalent noise charge as a function of the total radiation dose. Rectangle, circle and triangle points indicate VA chip with no input load capacitance, 20 pF and 51 pF load capacitance, respectively. The initial noise (ENC) offset and slope were 194 e^- and 7.19 e^-, respectively. Both noise offset and slope increased almost linearly with radiation dose. They were 429 e^- and 22.1 e^-/pF, respectively, after 100 krad of irradiation.

Fig. 4.4 shows gain degradation of VA chip as a function of the total radiation dose. The rate of the gain drop was 0.3 %/ krad and the load capacitance had no effect on gain drop with any radiation dose.

The VA1 chip has several adjustable parameters to properly operate the shaper and the preamplifier. Table 4.1 and figure 4.5 show the VA1 bias pa-

[1] While shaping time will be set to 2.5 μsec in a real operation, we could not set it properly due to the repeater system then available.

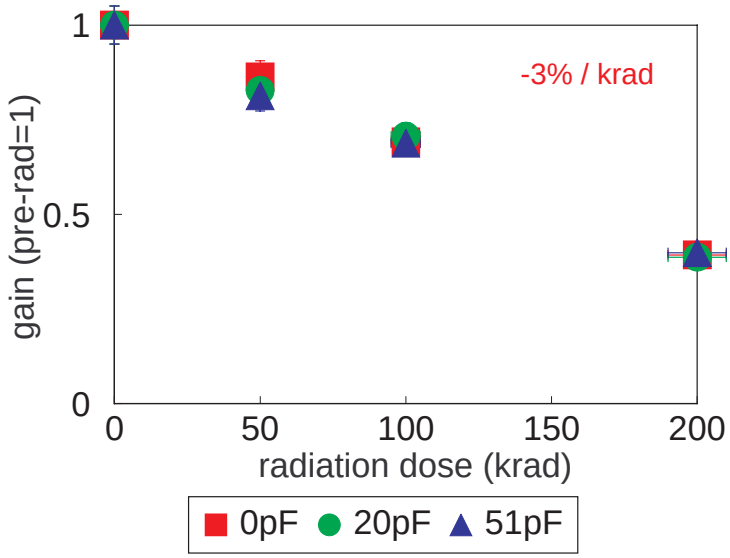

Figure 4.4: Gain degradation of VA1 chip as a function of radiation dose

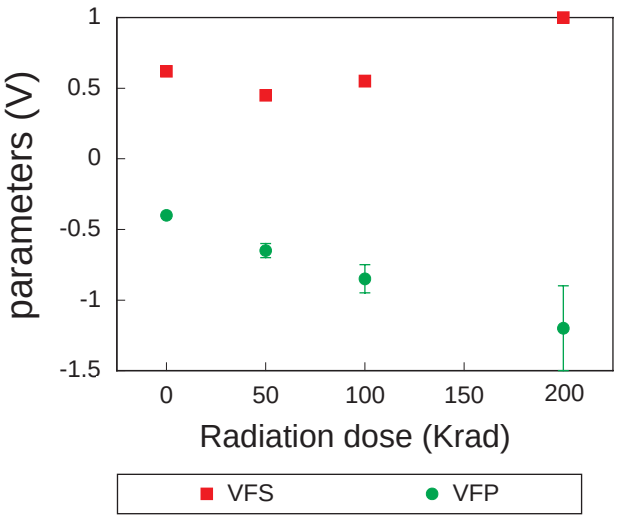

Figure 4.5: Vfp, Vfs vs. radiation dose. Bars of Vfp data points represent the region in which ENC does not change

Table 4.1: The VA1 bias parameters

parameter	value
I_buf	200 mV
Sha_bias	-790 mV
Pre_bias	440 mV
Vfs,Vfp	see Fig. 4.5

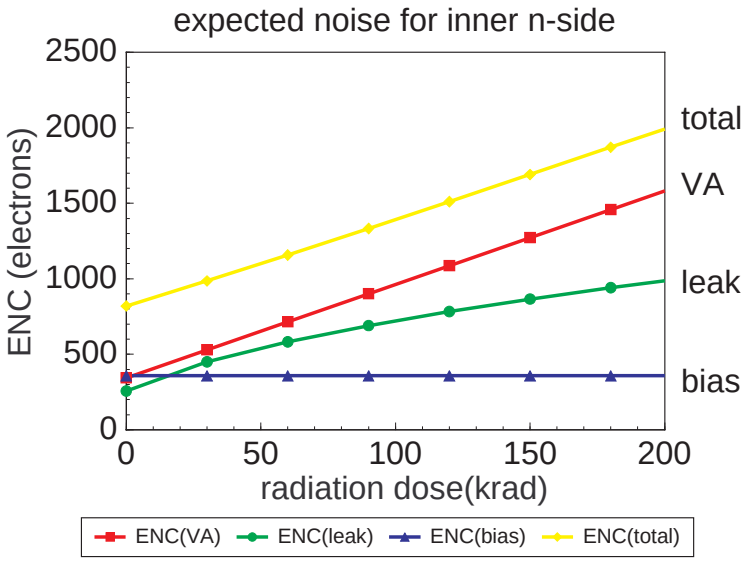

Figure 4.6: Noise performance of inner layer n-side

rameters for this measurement. We found some of these parameters need to be adjusted to keep proper shaping time and minimize the noise when irradiated.

In our measurement, two parameters were readjusted in each time. The Vfp was tuned to minimize the ENC, while Vfs was tuned to keep the same peaking time as its initial value, 1.7 μsec.

Power consumption does not change before/after irradiation.

4.2.3 Signal to Noise Ratio

Based on above measurements and other information, total noise performance was calculated as a function of total radiation dose. For example, expected noise contributions from various sources of inner layer n-channel are shown in Fig. 4.6.

In Fig. 4.7, calculated S/N for each layer is shown as a function of the radiation dose at innermost layer. In this calculation, it is assumed that signal is 16500 e^- and the radiation dose is inversely proportional to the distance from the interaction point. Before irradiation, S/N of all three layer is above 15, decreasing to about 10 after 150 krad of irradiation. The minimum S/N required

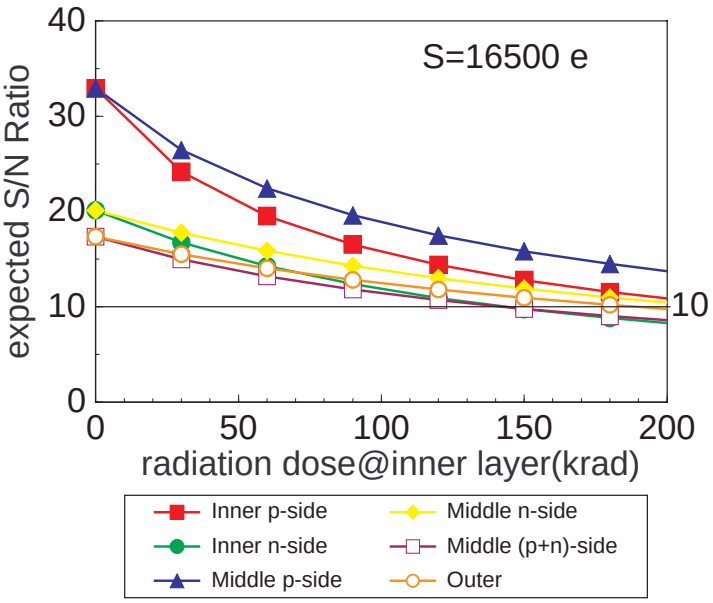

Figure 4.7: Expected S/N ratio of SVD as a function of radiation dose

for proper cluster-finding (especially on the z-side) in our configuration and readout scheme is about 10 from experience at the CLEO 2.5 SVX. Therefore, it is concluded that current SVD can withstand 150 krad of irradiation, which corresponds to 5 years of operation at the design luminosity of KEKB (if our assumption is correct).

4.3 Alignment Precision

Misalignment of detectors affects the vertex resolution. Alignment precision inside each ladder is determined by the accuracy of fixture fabrication, detector dicing and assembly operations. The torelance for assembly precision was set to 100 μm for shifts from designed position and 1 mrad for rotation angles. We studied the alignment precision using mechanical dummies before starting real production.

After each ladder mounted on end rings, its position was measured using optical measurement system. Table 4.2 shows the shift from designed position along the long boundary of DSSD, in the unit of mm. The mean values indicate the precision of fixture fabrication and the r.m.s. values represent the assembly variation. Total shifts were within the torelance (100 μm) and r.m.s. were about 20 μm for all the layer.

Table 4.3 shows the rotation angle between designed and measured position of each DSSD around the axis perpendicular to the DSSD plain, in the unit

Table 4.2: Shift from designed position along long boundary of DSSD (mm)

	DSSD 1	DSSD 2	DSSD 3	DSSD 4
ladder 0	0.0380	0.0770		
ladder 1	0.0300	0.0590		
ladder 2	0.0280	0.0530		
ladder 3	0.0450	0.0630		
ladder 4	0.0110	0.0180		
ladder 5	0.0310	0.0440		
ladder 6	0.0310	0.0600		
ladder 7	0.0300	0.0410		
layer1 mean	0.0305	0.0519		
layer1 r.m.s.	0.0090	0.0166		
ladder 8	0.0380	0.0190	0.0450	
ladder 9	0.0430	0.0210	0.0480	
ladder 10	0.0820	0.0640	0.0740	
ladder 11	0.0840	0.0660	0.0770	
ladder 12	0.0380	0.0220	0.0530	
ladder 13	0.0220	-0.0090	0.0040	
ladder 14	0.0500	0.0320	0.0610	
ladder 15	0.0450	0.0290	0.0660	
ladder 16	0.0570	0.0390	0.0510	
ladder 17	0.0620	0.0460	0.0650	
layer2 mean	0.0521	0.0329	0.0544	
layer2 r.m.s.	0.0186	0.0212	0.0197	
ladder 18	0.0200	0.0410	0.0140	0.0480
ladder 19	0.0140	0.0310	0.0120	0.0510
ladder 20	0.0400	0.0680	0.0390	0.0780
ladder 21	0.0630	0.0870	0.0710	0.0920
ladder 22	0.0200	0.0370	0.0120	0.0400
ladder 23	0.0260	0.0350	0.0200	0.0470
ladder 24	0.0370	0.0530	0.0560	0.0760
ladder 25	0.0440	0.0490	0.0390	0.0590
ladder 26	0.0550	0.0920	0.0890	0.1070
ladder 27	0.0410	0.0530	0.0310	0.0570
ladder 28	0.0070	0.0170	0.0060	0.0370
ladder 29	0.0450	0.0610	0.0490	0.0730
ladder 30	0.0140	0.0180	0.0170	0.0560
ladder 31	0.0320	0.0450	0.0230	0.0630
layer3 mean	0.0327	0.0491	0.0341	0.0631
layer3 r.m.s.	0.0160	0.0216	0.0238	0.0193

Table 4.3: Rotation angle around the axis perpendicular to the DSSD surface (radian)

	DSSD 1	DSSD 2	DSSD 3	DSSD 4
ladder 0	-1.020E-4	-1.220E-3		
ladder 1	-5.840E-4	-1.170E-3		
ladder 2	-7.670E-4	-1.160E-3		
ladder 3	-7.230E-4	-1.330E-3		
ladder 4	-5.980E-4	-1.140E-3		
ladder 5	-1.470E-3	-1.680E-3		
ladder 6	-9.690E-4	-1.630E-3		
ladder 7	-7.440E-4	-1.310E-3		
layer1 mean	-7.446E-4	-1.330E-3		
layer1 r.m.s.	3.602E-4	1.986E-4		
ladder 8	1.080E-5	4.740E-4	-1.030E-4	
ladder 9	-2.420E-4	2.980E-4	-3.280E-4	
ladder 10	-5.570E-4	-1.940E-4	-7.220E-4	
ladder 11	-5.270E-4	9.720E-4	8.080E-4	
ladder 12	2.520E-4	9.100E-4	3.320E-4	
ladder 13	-6.350E-4	-4.740E-4	-7.270E-4	
ladder 14	-6.000E-4	-1.080E-4	-5.660E-4	
ladder 15	-4.210E-4	8.120E-5	-5.000E-4	
ladder 16	-2.670E-4	6.610E-4	-4.000E-4	
ladder 17	2.680E-4	7.200E-4	1.730E-4	
layer2 mean	-2.718E-4	3.340E-4	-2.033E-4	
layer2 r.m.s.	3.248E-4	4.697E-4	4.773E-4	
ladder 18	-4.320E-4	-4.200E-4	-1.200E-4	1.340E-5
ladder 19	1.500E-4	-1.350E-4	3.210E-4	-3.120E-4
ladder 20	-5.490E-4	-1.040E-3	-1.910E-4	-4.810E-4
ladder 21	-6.390E-4	1.830E-4	9.110E-4	5.810E-4
ladder 22	-9.120E-4	-5.690E-4	-9.530E-5	-3.500E-4
ladder 23	-7.170E-4	-3.500E-4	-6.960E-5	-2.850E-4
ladder 24	-1.050E-3	-8.700E-4	-7.300E-4	-4.050E-4
ladder 25	-1.420E-5	-1.610E-4	5.610E-4	4.270E-5
ladder 26	-4.060E-4	-5.810E-4	-3.740E-4	-6.140E-4
ladder 27	4.570E-5	-4.520E-4	-7.290E-5	-5.310E-4
ladder 28	-2.840E-4	-2.680E-4	-2.190E-5	-1.520E-4
ladder 29	-6.210E-4	-9.210E-4	-6.280E-4	-1.050E-3
ladder 30	-7.580E-4	-4.430E-4	-3.410E-4	-6.070E-4
ladder 31	-1.090E-3	-6.720E-4	-2.670E-4	-1.250E-4
layer3 mean	-5.197E-4	-4.785E-4	-7.984E-5	-3.053E-4
layer3 r.m.s.	3.762E-4	3.211E-4	4.212E-4	3.683E-4

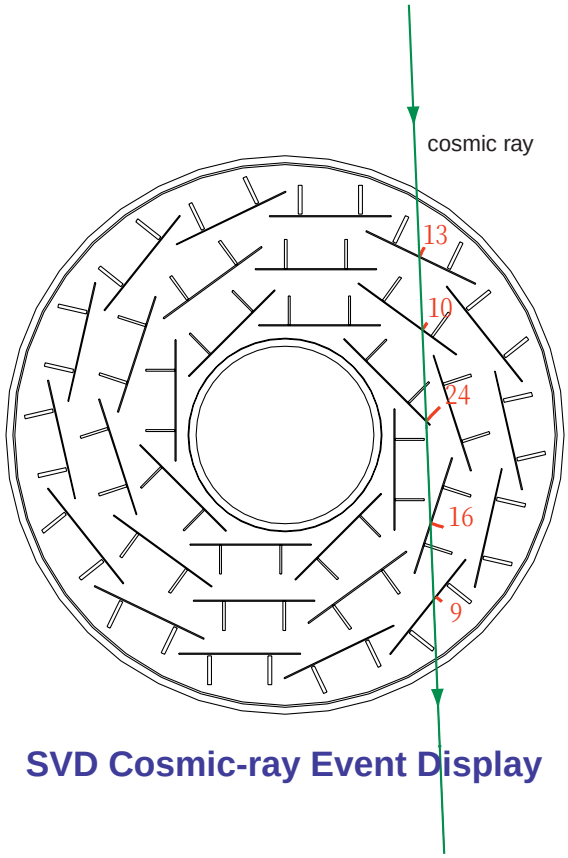

Figure 4.8: A cosmic ray event reconstructed by SVD. The length of bars is proportional to the size of signal, which is also indicated by number in the unit of 1000 electrons.

of radian. The assembly precision (r.m.s. value) was better than torelance (1 mrad) for all the layer.

More precise study of alignment of each DSSD is now going on and the alignment constants will be determined using data from cosmic ray and real run.

4.4 Cosmic Ray Test

During system integration test carried out on Oct. and Nov. 1998, cosmic ray signal was detected. Coincidenced scintilation counters provided trigger information necessary for read out. Fig. 4.8 shows an r-ϕ view of a cosmic event. The DSSDs and the support ribs are shown. The hits on DSSDs are indicated by bars perpendicular to the DSSDs. The numbers nearby the hit bars indicate the size of signal in the unit of 1000 electrons. Cosmic ray track was reconstructed from hit information and also shown in the figure.

Figure 4.9, 4.10 and 4.11 show measured pulse height distribution (in the unit of electron) of cosmic ray events for p, n and (n+p) channels, respectively.

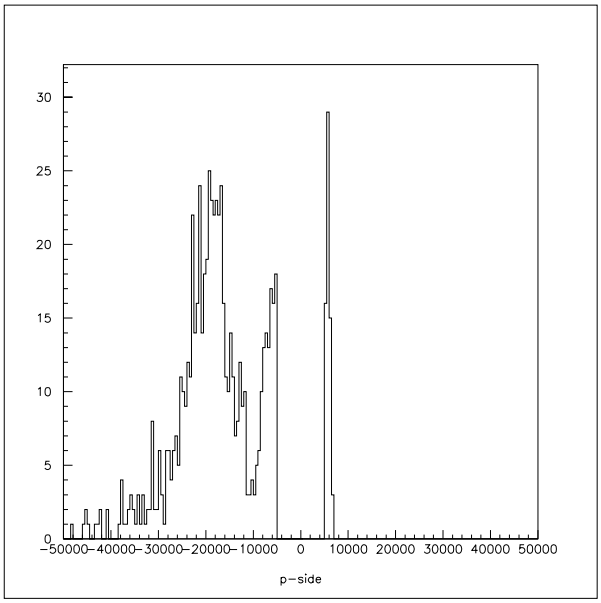

Figure 4.9: Pulse height distribution for p-side

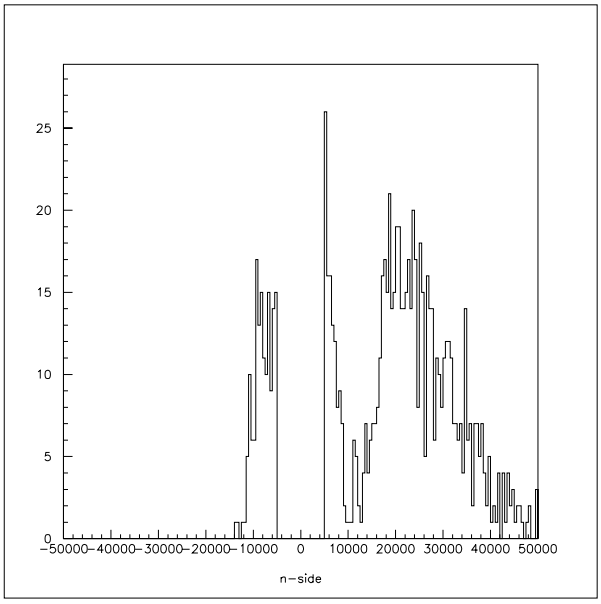

Figure 4.10: Pulse height distribution for n-side

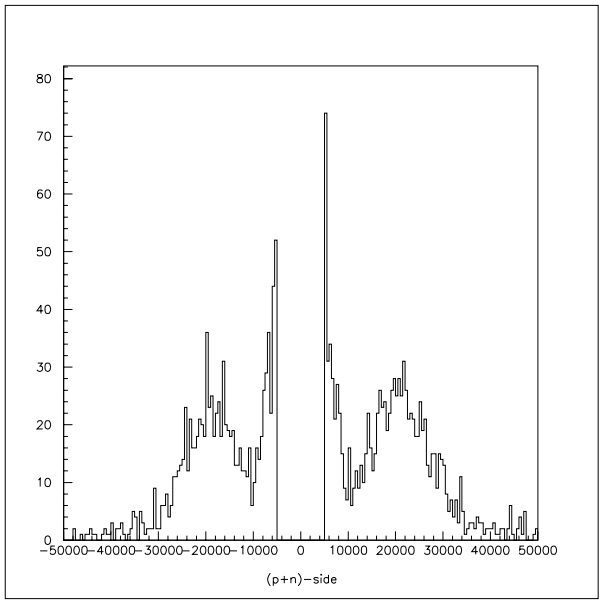

Figure 4.11: Pulse height distribution for (p+n)-side

Clusters which pulse height are below 5000 e^- are not taken into account to eliminate noise hits. The peaks seen just above 5000 $e-$ are due to noise.

Since calibration of preamplifier gain and tuning of various parameters were not sufficient, the absolute values are not significant. However, S/N ratio gives us some information about the performance of the detector system. The peak of measured signal pulse height was $\sim$ 20000 e^- in each type of detector. Measured average noise for n, p and (n+p) channels at this measurement are 500–700 e^-, 1000–1200 e^- and 1000–1300 e^-, respectively. Therefore, S/N ratios for n, p and (n+p) channels were 28-40, 17-20 and 15-20, respectively. These values are consistent with expected S/N ratios.

4.5 Comments for Future Upgrade

It was pointed out that the current SVD system has some shortcomings. The greatest shortcoming is the radiation torelance of its frontend electronics. In the background estimation, we assumed the vacuum of 1 nTorr, which is difficult to achieve in the real operation. Taking this into account, safety factor of at least 5 is needed.

Another shortcoming is its geometry. Angular acceptance of current SVD is 0.87 in the center of mass frame, while that of CDC is 0.92, 6% larger than the SVD. As a result, part of mechanical structure of the SVD (especially heatsinks) are located inside the tracking volume, which makes the tracking resolution worse.

The next version of the SVD must be constructed to improve these shortcomings. The frontend electronics should withstand at least 500 krad of irradiation. The angular acceptance should be the same as that of the CDC in order to reduce the material inside the tracking volume.

Chapter 5

Conclusion

The BELLE Silicon Vertex Detector (SVD) was designed to provide vertex information necessary for the study of CP violation in the decays of B mesons, which is the main purpose of the BELLE experiment.

The SVD is required to measure the vertices of B mesons better than 100 μm and to withstand under the high radiation environment for several years. The configuration of the SVD was determined to satisfy these requirements. The SVD consists of three cylindrical layers placed between 30-60 mm from the interaction point. Each layers are constructed from independent detector modules, which called as *ladders*.

Major problem during assembly was punch-through strips in the coupling capacitor of detectors which makes the neighboring channels very noisy. We found potential punch-through by burn-in performed after wire-bonding and before full-ladder assembly. The wires connected to punch-through strips were removed. All the ladders necessary for experiment were assembled successfully. The strip yield was better than 97% for the inner layer ladders and better than 90% for all the ladders.

The vertex (Δz) resolution of the constructed SVD was estimated by Monte Calro simulation to be 97 μm, which satisfies the requirement. The radiation tolerance was measured to be sufficient for operation at KEKB for five years under assumption of 1 nTorr vacuum. Cosmic ray signals were detected and the data was analyzed. The calculated S/N ratio indicates that the performance of the constructed SVD is as expected.

Appendix A

Principle of Silicon Strip Detector

Semiconductor detectors, originally used for energy measurement of ionizing particles in nuclear physics, are now widely used in particle and nuclear physics experiments. In particular, their capability of precise position measurement makes silicon detectors very popular device in particle physics experiment in which accurate position measurement is necessary.

In this chapter, the fundamentals of semiconductor devises and the principle of silicon strip detector are described.

A.1 Semiconductor Device Basics

In a perfect crystal, electron energies are constrained to lie in bands. The valence band and conduction band are separated by an energy gap in which no electrons are allowed. Electrons in valence band are excited thermally to conduction band. Electrons missing in the valence band are called holes. For an intrinsic semiconductor, the number of electrons is equal to the number of holes.

Semiconductors are usually doped with small fraction of impurities to produce additional states in the originally forbidden energy gap. The impurity atoms with one additional electron in the outer shell (e.g. phosphorus or arsenic) are called "donor" and those with one less valence electron (e.g. boron in silicon) called "acceptor". In n-type (doped with donor atoms) semiconductors, almost all electrons from donor states situated close to conduction band will move into the conduction band because of the high density of available free states in the band. This causes a shift of the Fermi level from the gap center toward the conduction band and a decrease in the density of holes in the valence band. In p-type (doped with acceptor atoms) materials, an increase of hole densities and a decrease of electron densities are caused by similar effects.

A.1.1 p-n Junction

Band structures of p and n semiconductors are shown in Fig.A.1(a). Once they are brought into contact, electrons and holes drift into the p-region and the

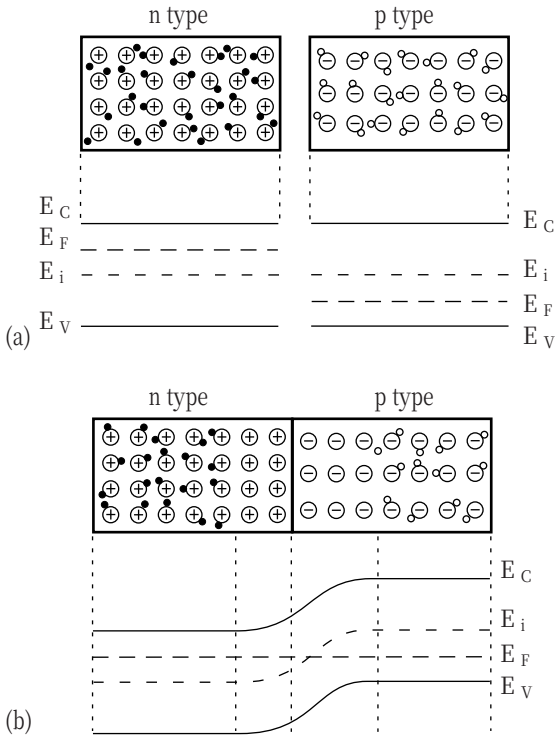

Figure A.1: p-n junction

n-region, respectively. This causes an excess of negative charge in the p-region and positive charge in the n-region. As a result, electric field is created and any movable charge carriers (electrons and holes) are swept out from the region around the boundary, resulting in a space charge region (Fig.A.1(b)).

If negative voltage on n-side and positive voltage on p-side are applied, movable charge carriers are pushed toward the junction, electrons and holes recombine near the interface and current flow. When the voltage in the opposite direction is applied, electrons and holes are pulled away and the space charge region increases.

A.1.2 MOS structure

MOS(Metal-Oxide-Semiconductor) devises are also widely used and are of great importance.

Consider n-type semiconductor as an example. If an external voltage is not applied to the metal, the electrons will be uniformly distributed in the semiconductor, and the electric field will be zero anywhere in the device (Figure A.2 1). If a positive voltage is applied to the metal with respect to the semiconductor bulk, electrons will be attracted to the semiconductor oxide interface, and a thin layer of negative charge will form in the semiconductor at the boundary (Figure A.2 2). A voltage will then appear across the oxide layer. This process is called as accumulation and the negative charge layer is called as accumulation layer.

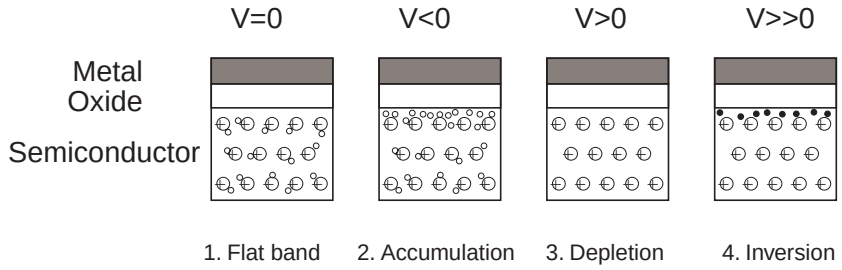

Figure A.2: A schematic drawing of MOS structure

The situation is more complex if a negative voltage is applied to the metal. This causes the electrons to be repelled from the interface and positively charged space region will form. If the voltage is small, this situation is stable and is called depletion (Figure A.2 3). If the voltage is further increased, the depletion width will increase (usually proportional to the square root of the voltage). Thermally generated electron-hole pairs will be separated by the electric field in the space charge region, with the electrons moving toward the bulk and the holes accumulating at the semiconductor-insulator interface. The resulting thin positive charge layer is called as the inversion layer (Figure A.2 4).

MOS FET(Field Effect Transistor) consists of three terminals, source(S), drain(D) and gate(G) on the substrate, as shown in Fig. A.3. The portion of the semiconductor under the gate connecting the source and the drain is called channel region. For *enhancement* mode MOSFET, current does not flow when no external voltage is applied. When voltage is applied between the source and the gate(V_{GS}) in such direction as inversion layer forms in the channel, current flows between the source and the drain terminals. Since the concentration of the carriers in the channel increases with increasing V_{GS}, the magnitude of current for a given drain voltage can be controlled by V_{GS}. Depending on the type of carriers flowing in the channel, MOSFET is classified as either an n-channel (electron conduction) or p-channel (hole conduction) type device.

A.1.3 Radiation Effects on MOS Structure

When semiconductor devises are exposed to ionizing radiation, they are damaged in various way. MOS devices are damaged mainly in two ways: increase of oxide trap and interface trap.

When an ionizing particle penetrates the oxide layer of MOS structure, it produces electron hole pairs. Although the electrons move quickly outside of the oxide, the holes move slowly and some of them may eventually trapped by oxide. These oxide-trapped charge tends to trap and detrap the carriers near oxide-substrate interface. This causes fluctuation of the number of carriers and leads to increase in 1/f noise of a MOS transistor. Because of increase in positive charge in oxide layer, oxide trap also causes a negative shift in V-I characteristic of MOS devices.

Holes generated inside the oxide layer move toward the interface between the oxide layer and the substrate. They may also trap electrons and form new localized electric states with energy level near conduction or valence band edge. The interface trap states are classified into two types by their nature.

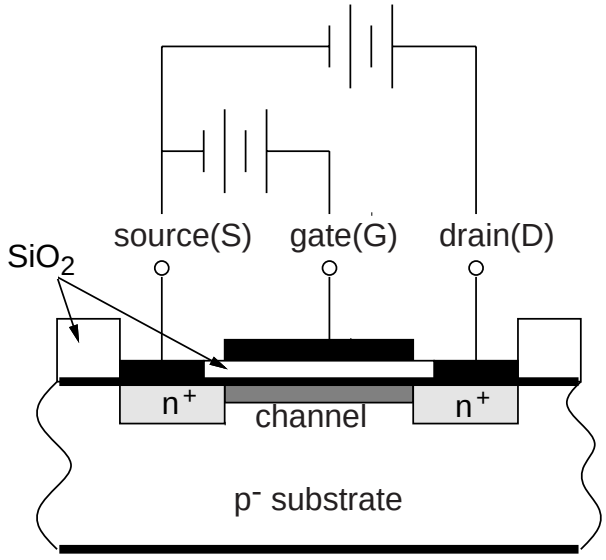

Figure A.3: The structure of MOS FET

When the level is near valence band edge, it releases an electron and becomes positively charged (a donor-like trap). When the level is near conduction band edge, it captures an additional electron and becomes negatively charged (an acceptor-like trap). The interaction between interface traps and carriers causes the mobility degradation, which decreases transconductance and increases white noise of MOS FET.

A.2 Silicon Strip Detector

Strip detectors are in principle large area diode divided into narrow strips, each of which is read out by a separate electronic circuit. The detector consists of a highly doped p^+ region on a low doped n^- substrate, the backside of a highly doped n^+ layer. Usually, reversed bias is applied to fully deplete the substrate, making sensitive area wider and number of produced charge greater.

Charged particles passing through the detector ionize atoms in the depletion region to produce electron-hole pairs. Generated electrons and holes are separated by the strong electric field and electrons (holes) will drift towards n^+ (p^+) electrode. The position of charged particle is given by the location of the strip carrying the signal.

The signal from detector is read out as amount of charge collected in the electrode. It is converted into voltage by a charge amplifier and sent to ADC.

The nominal thickness of a silicon strip detector is 300μm and the energy necessary to produce an electron-hole pair is 3.6 eV in silicon. Minimum ionizing particle deposits about 80 keV of its energy into 300μm thick Si detector and creates about 22000 electron-hole pairs. Since the charge collection efficiency of the SSD is reported to be 0.8[9], total collected charge would be about 17000 e.

Single-sided strip detectors described above make use of only one type of charge carrier, usually holes. By dividing the backside n^+ layer into strips

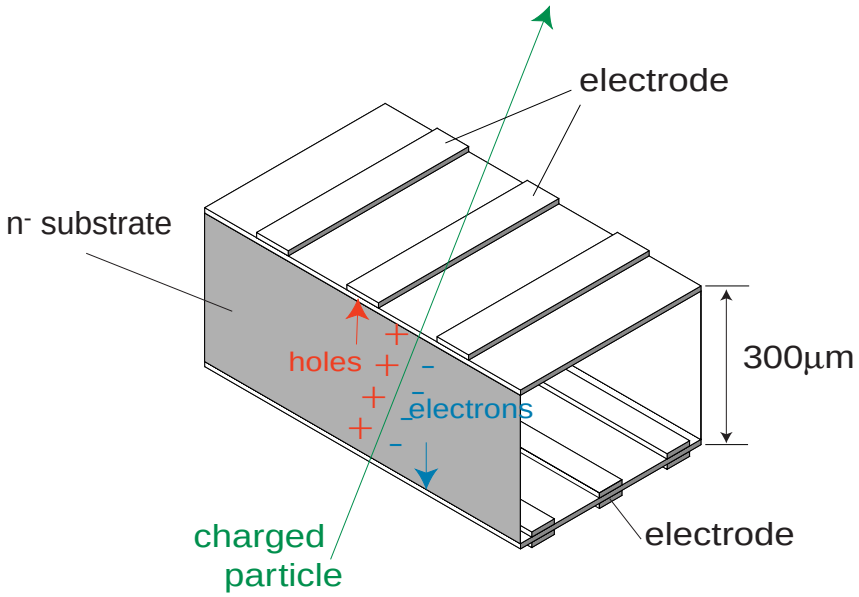

Figure A.4: A schematic drawing of Double-sided Silicon Strip Detector(DSSD).

and using electrons collected there, a second coordinate can be read out from the same wafer. (Fig. A.4) This is the principle of double-sided silicon strip detector (DSSD). Since two-dimensional information can be obtained by one silicon wafer, one can reduce effects of multiple scattering by using DSSD.

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Bibliography

[1] J. H. Christenson *et al.*, *Phys. Rev. Lett.* 13, **138** (1964)

[2] M. Kobayashi and T. Maskawa, *Prog. Theo. Phys.* **49**, 652 (1973)

[3] BELLE collaboration, "Technical Design Report for the BELLE Detector", KEK Report 95-1(1995)

[4] BELLE SVD Group, "Technical Design Report of BELLE SVD" (1998)

[5] T. Kawasaki, "Test of double length DSSD", BELLE Note #66, Apr. 1995

[6] M. Yokoyama and H. Tajima, "Measurement of radiation effects on VA1 chip", BELLE Note #196, Dec. 1997

[7] M. Yokoyama, Talk at SVD II workshop, May 1998

[8] A. D. Foland *et al.*, "Radiation-induced Surface Leakage Current in Silicon Microstrip Detectors", *IEEE Trans. Nucl. Sci.* **44** (1997)

[9] J. P. Alexander *et al*, *Nucl. Inst. Meth.* **A342**, 282 (1994)