Research and Development of the Silicon Vertex Detector Trigger for the Belle Experiment

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Abstract

A new silicon strip readout chip, the VA1TA, is developed for the upgraded Silicon Vertex Detector (SVD) of the Belle experiment. The VA1TA chip is designed to add a trigger capability to the SVD. The noise of the analog output with a DSSD connected is measured to be 520 e^- for peaking time = 0.7 μs. This corresponds to the S/N ratio of 36. The threshold of the trigger discriminator can be set to as low as 5000 e^- with a peaking time of 75 ns by optimizing the bias parameters. The VA1TA provides a fast trigger signal for less than 75 ns after the event occurred.

We conclude that the performance of the VA1TA chip is satisfactory for the upgraded SVD of the Belle experiment.

Contents

Chapter 1

Introduction

CP violation has been one of the central concerns of particle physics since its discovery in K meson system in 1964 [1]. In 1973, M. Kobayashi and T. Maskawa (KM) proposed a theory that can introduce CP asymmetry within the framework of the Standard Model [2]. In 1980, Sanda and Carter pointed out that the KM model contains a possibility of rather sizable CP violating asymmetries in certain decay modes of the B mesons [3]. The observation of the CP violation in B meson decays would be a confirmation of the KM model. The Belle experiment has been built to verify the KM model in KEK.

Decays of B^0-$\overline{B}^0$ pair originating from the $\Upsilon(4S)$ into a CP eigenstate f_{CP} produce CP-violating asymmetries A_{CP} given by

$$A_{CP}(\Delta t) = \frac{\Gamma(B^0 \to f_{CP}) - \Gamma(\overline{B}^0 \to f_{CP})}{\Gamma(B^0 \to f_{CP}) + \Gamma(\overline{B}^0 \to f_{CP})} = \sin(2\phi_{CP}) \sin(\Delta m \cdot \Delta t), \qquad (1.1)$$

where $\sin(2\phi_{CP})$ is a parameter related to the KM model, Δm denotes the mass difference between the two B^0 mass eigenstates, and $\Delta t \equiv t_2 - t_1$, where t_1 and t_2 are the proper time for the $B \to f_{CP}$ decay and for the associated B decay, respectively. The Δt value range is $-\infty$ to $+\infty$ and the asymmetry vanishes in the time integrated rate. Therefore, a determination of Δt is required for the observation of a CP asymmetry.

We generate $\Upsilon(4S)$ at the KEKB asymmetric energy collider of e^+e^- beams. The $\Upsilon(4S)$ is produced with a constant motion along the beam direction (z axis). Because the B mesons are produced almost at rest in the center-of-mass system of $\Upsilon(4S)$, they also fly with the constant momenta along with z-axis. Δt is approximately calculated as

$$\Delta t \simeq \Delta z/(\beta\gamma_B)c, \qquad (1.2)$$

where Δz is a distance of the decay vertices of the B mesons in z, and $\beta\gamma_B$ is a Lorentz boost factor that is ~ 0.425 in our configuration. Since the typical decay distance of the B mesons is 200 μm, precise vertex detection is an essential feature of the detector. To this end we have built the silicon vertex detector (SVD).

We have achieved the Δz resolution of ~ 200 μm by the present SVD, which enabled us to observe large CP violation in the neutral B meson system [4]. However, whether the CP violation parameter is consistent with the theoretical prediction by the Kobayashi-Maskawa model is not yet conclusive. To determine the CP violation parameter even more precisely, more accurate vertex measurement and higher luminosity are required. We, therefore, upgrade the current Belle detector.

The current SVD consists of three cylindrical vertex detection layers. To improve the vertex resolution, we replace the innermost part of the drift chamber that provides z trigger with one more detection layer of the SVD. Because we anticipate the increased beam backgrounds with the higher luminosity, we need to develop an elaborate trigger based on the SVD signals.

A study shows that the SVD trigger discards background events efficiently than the z trigger [5]. In this thesis, we investigate the capability of the new trigger device of the upgraded SVD.

This thesis is organized as follows. We describe the CP violation in the B meson system in Chapter 2, and the current Belle detector in Chapter 3. The description of the SVD upgrade especially for the trigger system is given in Chapter 4. We study the trigger device in Chapter 5, and then Chapter 6 concludes this thesis.

Chapter 2

CP Violation

2.1 Introduction

Various symmetries play very important roles in particle physics. Some of them are continuous and the others are discrete. The CP symmetry is one of the latter and the origin of its violation is one of the most exciting mysteries in the present particle physics. As its name indicates, the CP transformation is a product of two discrete operations, C and P.

Charge conjugation, C, is a symmetry of the sign of particle charge. Parity, P, is a symmetry of space. P invariance means that the mirror image of an experiment yields the same result as the original.

Until 1956, it was believed that all elementary processes are invariant under C and P. Lee and Yang pointed out the possibility of the violation of these symmetries [6], and subsequent experiments [7] proved that C and P symmetries are really violated in weak interactions. However, the products of C and P transformations, CP was still a good symmetry.

The second impact came in 1964. An experiment using neutral K mesons showed that CP is also not conserved under weak interactions [1]. Neutral K mesons (K^0 and $\overline{K}^0$) are created by strong interactions. The mass eigenstates of the K^0 - $\overline{K}^0$ system can be written

$$|K_S\rangle = p|K^0\rangle + q|\overline{K}^0\rangle, |K_L\rangle = p|K^0\rangle - q|\overline{K}^0\rangle \tag{2.1}$$

(choosing the phase so that $CP|K^0\rangle = |\overline{K}^0\rangle$). If the CP invariance held, we would have $q = p$ so that K_S would be CP even and K_L would be CP odd. Because the kaon is the lightest strange meson, it decays through the weak interaction. Neutral

kaons can decay into two or three pions. Since a pion has CP eigenvalue of -1, K_S always decays into three pions, if CP is conserved in weak interactions. The experiment performed at Brookhaven proved that a small faction of K_L decays into two pions, which means CP is violated in the weak interaction. In the kaon system, the order of observed CP asymmetry is 10^{-3}.

2.2 Cabibbo-Kobayashi-Maskawa Matrix

In 1973, M. Kobayashi and T. Maskawa proposed a theory of quark mixing which can introduce the CP asymmetry within the framework of the Standard Model [2]. They demonstrated that the quark mixing matrix with a measurable complex phase introduces CP violation into the interactions.

In the Standard Model, the quark-W boson interaction part of the Lagrangian is written as

$$L_{qW} = \frac{g}{\sqrt{2}}\{\overline{u}_L \gamma_\mu W^+_\mu \mathbf{V} d_L + h.c.\}, \tag{2.2}$$

where g is the weak coupling constant, $u_L(d_L)$ represents the left-handed component of u-type (d-type) quarks, and $\mathbf{V}$ is the quark-mixing matrix.

If all the elements of the quark mixing matrix $\mathbf{V}$ are real, the amplitudes for a certain interaction and that for the CP conjugate interaction are the same. In order to violate the CP symmetry, $\mathbf{V}$ should have at least one complex phase as its parameter.

In general, N dimensional unitary matrix has N^2 parameters, with $N(N-1)/2$ real rotation angles and $N(N+1)/2$ phases. Since we can rephase the quark fields except one relative phase, $(2N-1)$ phases are absorbed and $(N-1)^2$ physical parameters are left. Among them, $N(N-1)/2$ are real angles and $(N-1)(N-2)/2$ are phases. The presence of the phases means that some of the elements must be complex and this leads to CP violating transitions.

In the case of $N = 2$, two quark-lepton generations, there is one rotation angle (the Cabibbo angle) and no phase. This means that CP must be conserved in the model with four quarks.

In the case of three generations, $N = 3$, there are three rotation angles and one phase so that CP can be violated. The quark mixing matrix for the six-quark model can be written in many parameterizations, but two parameterizations are especially

well known.

$$\mathbf{V} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \tag{2.3}$$

$$= \begin{pmatrix} c_{12}c_{13} & s_{12}c_{13} & s_{13}e^{-i\delta_{13}} \\ -s_{12}c_{23} - c_{12}s_{23}s_{13}e^{i\delta_{13}} & c_{12}c_{23} - s_{12}s_{23}s_{13}e^{i\delta_{13}} & s_{13}c_{13} \\ s_{12}s_{23} - c_{12}c_{23}s_{13}e^{i\delta_{13}} & -c_{12}s_{23} - s_{12}c_{23}s_{13}e^{i\delta_{13}} & c_{23}c_{13} \end{pmatrix} \tag{2.4}$$

$$\simeq \begin{pmatrix} 1 - \frac{1}{2}\lambda^2 & \lambda & A\lambda^3(\rho - i\eta) \\ -\lambda & 1 - \frac{1}{2}\lambda^2 & A\lambda^2 \\ A\lambda^3(1 - \rho - i\eta) & -A\lambda^2 & 1 \end{pmatrix}, \tag{2.5}$$

The first parameterization (2.4) is by Particle Data Group [8], where $c_{ij} \equiv \cos\theta_{ij}$ and $s_{ij} \equiv \sin\theta_{ij}$ for $i, j = 1, 2, 3$.

The second parameterization (2.5), originated by Wolfenstein [9], is also widely used. Setting λ to the sine of the Cabibbo angle [10], $\sin\theta_C \simeq 0.22$, and writing down all the elements in terms of powers of λ, the remaining three parameters are intended to be of order unity. It clearly indicates the hierarchy in the size of elements. The diagonal elements are almost unity. The elements between adjacent generations are smaller by an order of magnitude and the elements with the first and the third generations are further smaller. Experimentally, the parameters A and λ can be determined from tree-level decays and are rather well known [8]:

$$A = 0.84 \pm 0.04, \qquad \lambda = 0.2196 \pm 0.0023, \tag{2.6}$$

while ρ and η are not determined precisely, since their determination requires the measurement of V_{ub} and V_{td} which are of order λ^3.

The unitarity of the CKM matrix leads to some constraints on its elements. For example, the product between the first and the second columns lead to the equation,

$$V_{ud}V_{us}^* + V_{cd}V_{cs}^* + V_{td}V_{ts}^* = 0, \tag{2.7}$$

which is related to the K meson system. Since the elements of the CKM matrix are complex, this implies they form triangles on a complex plane. Although the unitarity of the CKM matrix leads to six triangles, most of them have one side which is much shorter than the other two sides, and consequently one tiny angle. In the Wolfenstein parameterization, we can compare the magnitudes of three terms in equation (2.7):

$$O(\lambda) + O(\lambda) + O(\lambda^5) = 0. \tag{2.8}$$

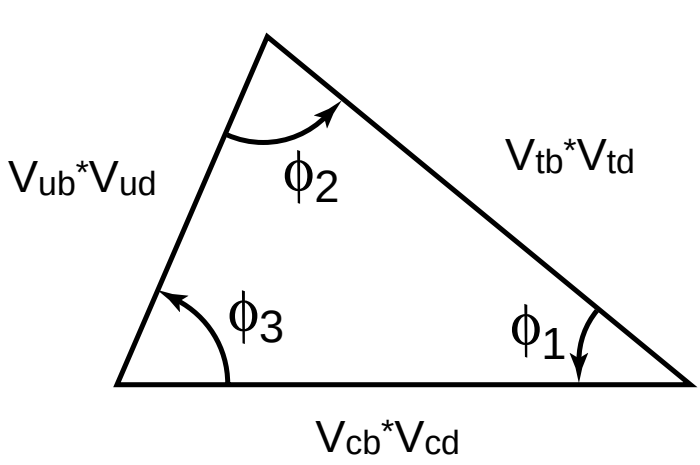


Figure 2.1: Unitary Triangle

This explains why the observed CP asymmetries in K decays, related to the tiny angle, are very small ($\mathcal{O}(10^{-3})$).

On the other hand, the B meson system is related to the following equation:

$$V_{ud}V_{ub}^* + V_{cd}V_{cb}^* + V_{td}V_{tb}^* = 0, \tag{2.9}$$

where all the three terms are the same order of magnitude, $O(\lambda^3)$. This implies that all the three angle can be large in the triangle related to Equation (2.9), which leads to the possibility of large observable CP asymmetries in the B meson decays. The triangle related to B meson system (illustrated in Fig. 2.1) is sometimes called the "Unitary Triangle".

Since the only two generations are related to the tree diagrams of the K meson decays, the sensitivity to the parameters related to the CP violation is limited in the K system. In B meson system, all the angle ϕ_1, ϕ_2 and ϕ_3 can be measured independently, which leads to precise tests of the Standard Model.

2.3 Measuring CP Asymmetry in B Meson Decays

B meson can be produced in two energy regions, a center-of-mass (CM) energy equal to or higher than the $\Upsilon(4S)$ mass.

There are some advantages in producing B mesons at the $\Upsilon(4S)$ energy region: The $B\overline{B}$ cross section is the highest in the all CM energy; B-$\overline{B}$ pairs are exclusively

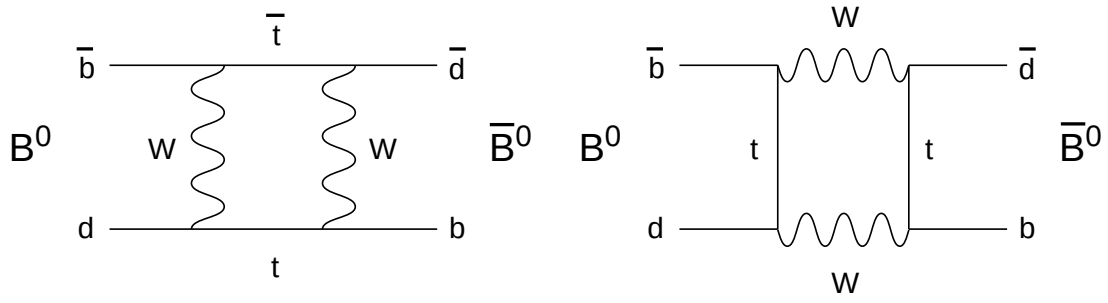


Figure 2.2: Feynman diagrams responsible for B^0-$\overline{B}^0$ mixing

produced (50% $B^0\overline{B}^0$ and 50% B^+B^-); The energy of the produced B meson is known, which can be used to reduce the combinatorial background.

One of the most promising methods to measure the CP angles in the B meson system is based on neutral B decays to CP eigenstates f_{CP}, which are common to B^0 and $\overline{B}^0$. B^0 and $\overline{B}^0$ can "mix" through the loop diagrams shown in Fig. 2.2, i.e. after a certain time, a meson B^0 at a production point is not a pure B^0 state, but a mixed state of B^0 and $\overline{B}^0$. The CP violation is induced by B^0-$\overline{B}^0$ mixing through the interference of the two decay amplitudes of B^0, $A(B^0 \to f_{CP})$ and $A(B^0 \to \overline{B}^0 \to f_{CP})$. In order to detect this CP violation, one must know, or *tag* the flavor of the particle (B^0 or $\overline{B}^0$) at a given time.

On the $\Upsilon(4S)$, tagging one B as a B^0 or a $\overline{B}^0$ identifies the other with certainty. Since both C and P eigenvalues of $\Upsilon(4S)$ is -1 and the decay of $\Upsilon(4S)$ is caused by strong interaction which conserves CP, the produced B-$\overline{B}$ should be in a CP eigenstate with eigenvalue of 1. Because the spin of $\Upsilon(4S)$ is 1 and that of B is 0, B^0 and $\overline{B}^0$ mesons are produced with the orbital angular momentum of 1, which means the P eigenvalue of B-$\overline{B}$ system is -1. This restricts the C eigenvalue to be -1 and a $B\overline{B}$ pair will remain in a coherent state as long as neither B has decayed. If one of them is detected to be $B^0(\overline{B}^0)$ at a moment, the other is inevitably $\overline{B}^0(B^0)$ at that time. This is extremely important for measuring the CP violation.

For example, consider one B^0 from $\Upsilon(4S)$ decays into semi-leptonic mode, like $B \to D^* l\nu$ ($l = e$ or μ), after t_1 from its production. If that particle was $B^0(= \overline{b}d)$ at t_1, the charge of the lepton is positive (see Fig. 2.3) and if it was $\overline{B}^0(= b\overline{d})$, the charge of the lepton is negative. The flavor of B meson which decays into CP eigenstate is determined by the flavor of the associated B meson. There are mainly two methods to tag the flavor of B. One is based on semileptonic B decays and the other is the

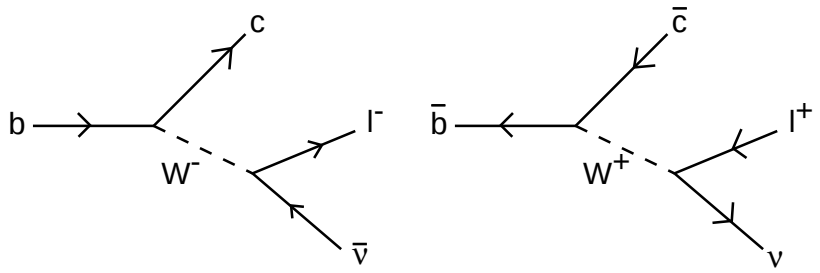


Figure 2.3: Feynman diagrams of semi-leptonic B^0 and $\overline{B}^0$ decays.

charge of the kaon from $b \to c \to s$ decay chain that also indicates the flavor of the B.

When a B^0-$\overline{B}^0$ pair is produced with an odd relative angular momentum, the rate for one of the neutral B mesons to decay as $\overline{B}^0$ at $t = t_1$ and the other (which is B^0 at $t = t_1$) to decay into a CP eigenstate, for example $J/\psi K_S$, at $t = t_2$ is written as

$$P\left(B^0 \to J/\psi K_S; \Delta t\right) = \frac{1}{2} e^{-\Gamma|\Delta t|}(1 + \lambda \sin \Delta m_d \Delta t), \tag{2.10}$$

where Γ is the B meson total decay width, $\Delta t \equiv t_2 - t_1$, Δm_d is the mass difference between the two weak eigenstates of neutral B mesons and λ is the CP asymmetry parameter

$$\lambda = -\sin(2\phi_1). \tag{2.11}$$

The CP conjugate of Eq. (2.10) is

$$P\left(\overline{B^0} \to J/\psi K_S; \Delta t\right) = \frac{1}{2} e^{-\Gamma|\Delta t|}(1 - \lambda \sin \Delta m_d \Delta t). \tag{2.12}$$

The value of Δt ranges from $-\infty$ to $+\infty$ and it is easily seen that the CP asymmetry vanishes in the time integrated rate. Therefore, the measurement of the decay time difference, Δt is required to observe the CP asymmetry in experiments at the $\Upsilon(4S)$.

In the normal e^+e^- colliders with identical energies of both e^+ and e^-, the $\Upsilon(4S)$ is produced at rest, and consequently the B mesons are produced at rest. Momenta of B's from $\Upsilon(4S)$ are about 325 MeV/c and the average decay length of the B's is about 30 μm, if the $\Upsilon(4S)$ is produced at rest. In this case, it is impossible to measure the time dependence with the present vertex detectors.

A solution is to produce the $\Upsilon(4S)$ moving in the laboratory frame. This can be achieved by colliding two beams of unequal energies. This results in two B mesons boosted in the same direction along the beam axis. The average distance between the

two B decays is approximately $\beta\gamma c\tau$ where $\beta\gamma$ is the boost parameter of the center of mass and τ is the average B lifetime. Since the B mesons move almost parallel to the beam axis, the decay time difference of two B mesons can be approximately calculated as

$$\Delta t \simeq \Delta z/\beta\gamma c, \tag{2.13}$$

where Δz is the distance between the decay vertices along the beam axis. A precise measurement of the decay vertices of the B mesons is necessary to measure the CP violation in this scheme.

Chapter 3

KEK B Factory

The primary goal of the KEK B factory experiment is the study of the CP violation in the B meson system. The KEKB accelerator is an asymmetric e^+e^- collider to produce B mesons. The decay products of B mesons are detected by the Belle detector. In Section 3.1, a brief introduction of the KEKB accelerator is given. In Section 3.2, the overview of the Belle detector and the description of its principal components are given.

3.1 KEKB Accelerator

As described in the previous section, to measure the CP asymmetry in decays of B mesons, we must produce $\Upsilon(4S)$'s boosted in the laboratory frame. The KEKB accelerator [11] was designed to realize this. It has two rings in a tunnel which was used for TRISTAN, one for the electron beam and the other for the positron beam. The circumference of the main rings is about 3 km. The configuration of the KEKB accelerator is shown in Fig. 3.1.

Beam energies are chosen to be 8.0 GeV for the electron and 3.5 GeV for the positron, so that the center of mass energy comes on the $\Upsilon(4S)$ resonance. In such configuration, $\beta\gamma \simeq 0.425$ and the average decay length of B mesons from the $\Upsilon(4S)$ is about 200 μm in the laboratory frame.

In order to produce as many B mesons as possible, the KEKB accelerator is designed to run at the highest luminosity in the world, 10^{34} cm^{-2}s^{-1}, corresponding to 10^8 $B\overline{B}$ pairs in a year. At the end of 2001, the KEKB has achieved a peak luminosity of 5.5×10^{33}cm^{-2}s^{-1}.

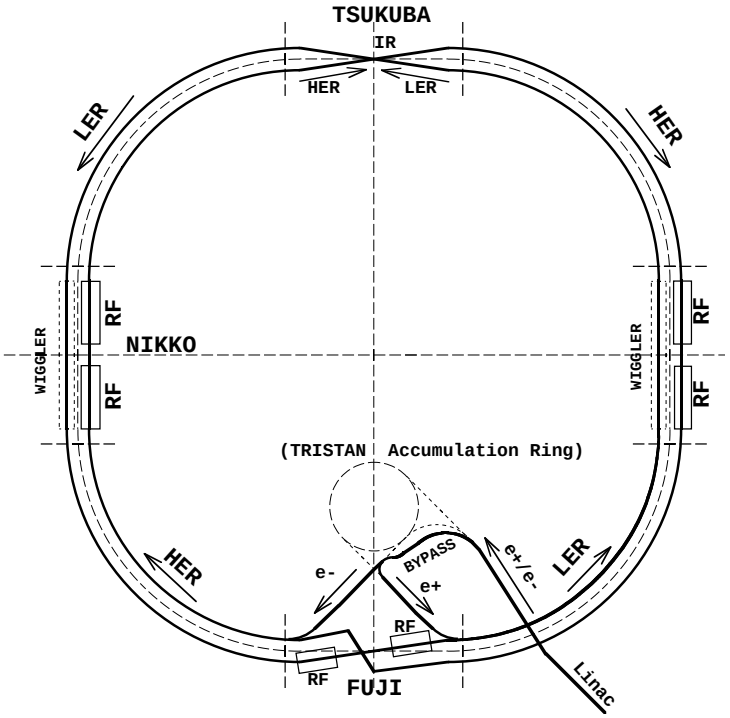


Figure 3.1: Configuration of the KEKB accelerator system

3.2 Belle Detector

The Belle detector (Fig. 3.2) is a 4π detector designed for the study of the CP violation in B meson system [12, 13]. The Belle detector consists of Silicon Vertex Detector (SVD), Central Drift Chamber (CDC), Aerogel Cherencov Counter (ACC) and Time of Flight counter (TOF), CsI calorimeter (ECL), and K_L and Muon detector (KLM).

Precise vertex measurement is provided by the SVD. Charged tracks are primarily reconstructed by the CDC. Electrons are identified by the CDC and ECL. Muons are identified by the KLM. The CDC, TOF and ACC provide K/π separations up to 3.5 GeV/c: the CDC covers the momentum up to 0.8 GeV/c, the TOF covers up to 1.2 GeV/c and the ACC covers momentum range 1.2 GeV/c< p < 3.5 GeV/c. Photons are detected by the ECL. K_L's are detected by the KLM.

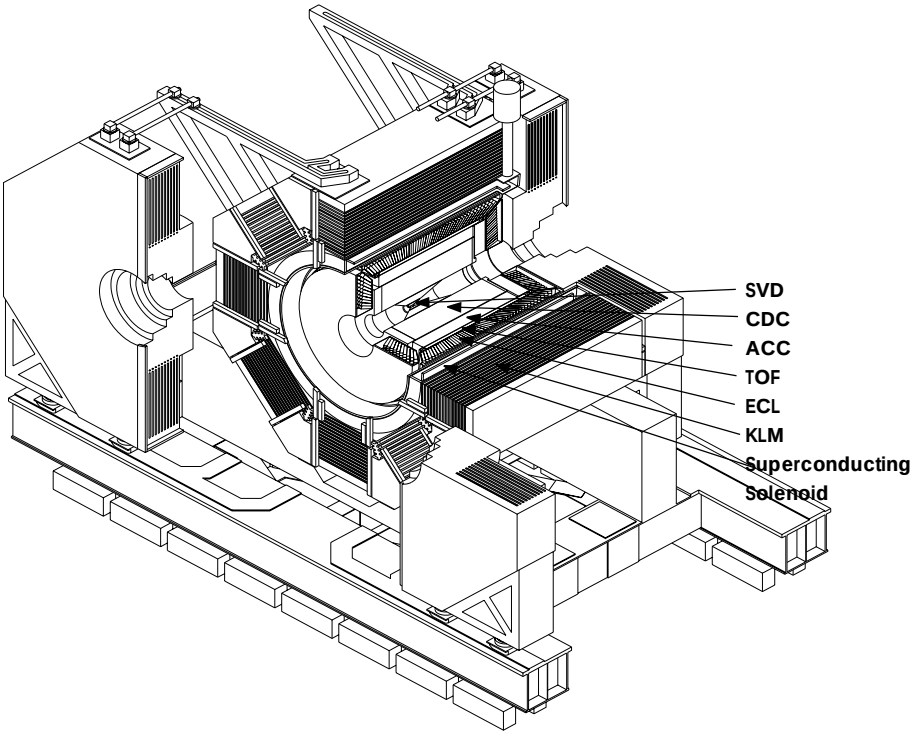


Figure 3.2: Schematic view of the Belle detector

3.2.1 Silicon Vertex Detector (SVD)

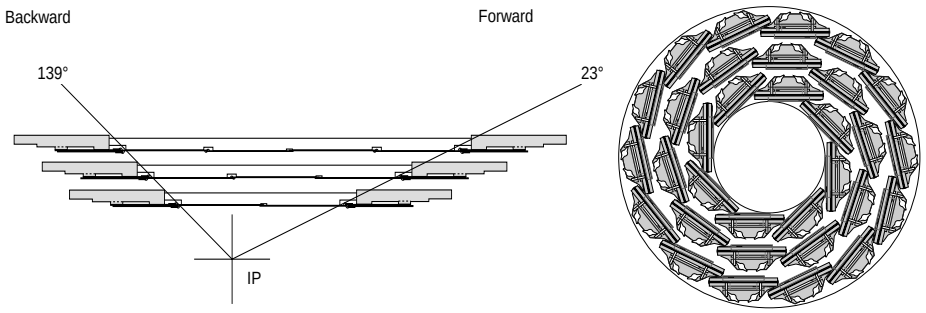
The main task of the Silicon Vertex Detector (SVD) [14] is to reconstruct the decay vertices of two B mesons in order to determine the time difference between two decays. The SVD is designed so that its position resolution is expected to be a few tens of μm, which is much better than the resolution of a wire drift chamber. The SVD is situated just inside the CDC and reconstructs precise tracks of charged particles combining the CDC measurement. The CDC can reconstruct low momentum tracks down to p_t about 70 MeV/c since the inner radius of the CDC is about 8 cm.

At the KEKB, the decay distance of $B\overline{B}$ pairs is about 200 μm in average. Therefore the target of the SVD vertex resolution was set to < 200 μm.

Multiple-Coulomb scattering is a dominant source of the vertex resolution degradation. This imposes strict constraints on the detector design and the mechanical layout. The innermost layer of the support structure must be low mass but stiff; and the readout electronics must be placed outside of the tracking volume.

3.2.1.1 Detector configuration

The SVD has three cylindrical layers consisting of units of the silicon sensors. The position of each layer is 3.0 cm, 4.55 cm and 6.05 cm in r radius, respectively. The SVD covers $23° < \theta < 139°$, corresponding to the angular acceptance of 86 %. The three layers have 8, 10 and 14 sensor ladders in ϕ. The structure of the SVD is shown in Fig. 3.3. Each layer is constructed from double-sided silicon strip detectors (DSSDs) and the front-end electronics.



(a) Side view (b) End view

Figure 3.3: Side and end views of the Belle SVD

DSSD We use the S6939 DSSD fabricated by HAMAMATSU Photonics. In a DSSD, p^+ and n^+-strips are formed on both side of substrate, perpendicular to each other. To avoid an interstrip conductivity between n^+-strips, p^+-strips are implanted between n^+-strips, which isolate the strips. These p^+ regions are called p-stop. The S6936 DSSD has 1280 sense strips and 640 readout pads on each side. All sense strips are biased via 25 MΩ polysilicon bias registers. The detector employs integrated AC coupling capacitors on both sides to capacitive signal readout from floating strips.

Ohmic (n^-) side is selected to be the z-side. In order to read out the signal of z-strips along the beam axis, an additional layer is formed on the top of and orthogonal to the z sensitive strips. This structure is called a double metal layer structure. The z-strip pitch is 42 μm and adjacent strips are connected to one readout trace on the second metal layer. The p-strip pitch is 25 μm and every other strips are connected to the readout pads.

The p-strips and n-strips detect electron-hole pairs which are induced by charged

tracks. The signal from the DSSD is read out as the amount of charge collected in the readout electrode. It is converted into the voltage by the preamplifier of the VA1. The thickness of the DSSD is 300 μm and the required energy to produce an electron-hole pair is 3.6 eV in the silicon. A minimum ionizing particle deposits about 80 keV of its energy into a 300 μm thick silicon detector and creates about 22000 electron-hole pairs. The measured most-probable peak height is approximately 19000 e^-, which corresponds to the charge collection efficiency about 86%.

3.2.1.2 Readout Electronics

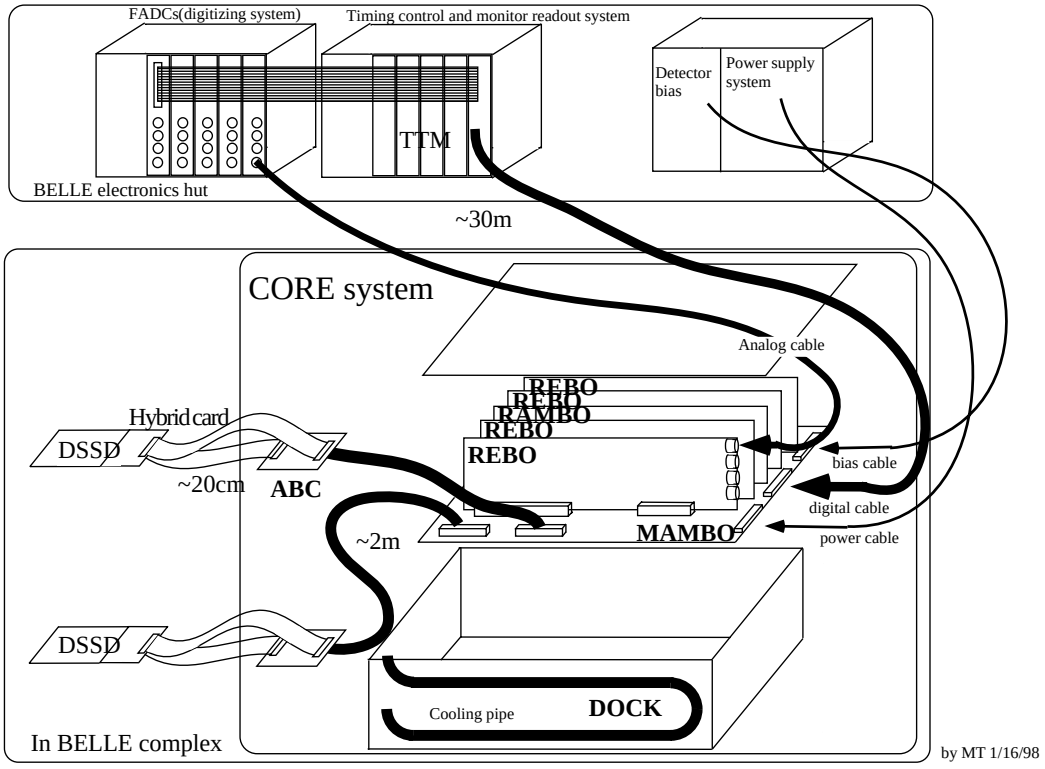


Figure 3.4: Block diagram of the SVD readout system

Figure 3.4 shows a block diagram of the overall readout system. The signals from the DSSD are read out by the VA1 chip mounted on the hybrid board and transferred via thin cables to a buffer card (ABC) followed by thicker cables and a repeater board (REBO). The REBO amplifies and retransmits (repeats) the received signal. The REBO drives a 30 m long cable to send a differential output to the receivers located in the electronics hut. Flash ADC (FADC) modules are installed in

the electronics hut to digitize the analog signals. Motorola DSPs embedded in the FADC module subtract pedestals from the digitized signals and compress the data size. The processed data are fetched and transferred to the central DAQ system by SPARC modules.

VA1 Chip The VA1 chip [15], which is originally developed at CERN and commercially available from IDEAS, Oslo, Norway, is used as a front-end readout chip. The VA1 is 128 channel CMOS integrated circuit designed for the readout of silicon vertex detectors and other small signal devices. It has extremely good noise performance (equivalent noise charge = 165 e^- + 6.1 e^-/pF with 2.5 μs shaping time) and consumes only 1.2 mV per channel. The VA1 is radiation tolerant to levels of order 200 kRad [16].

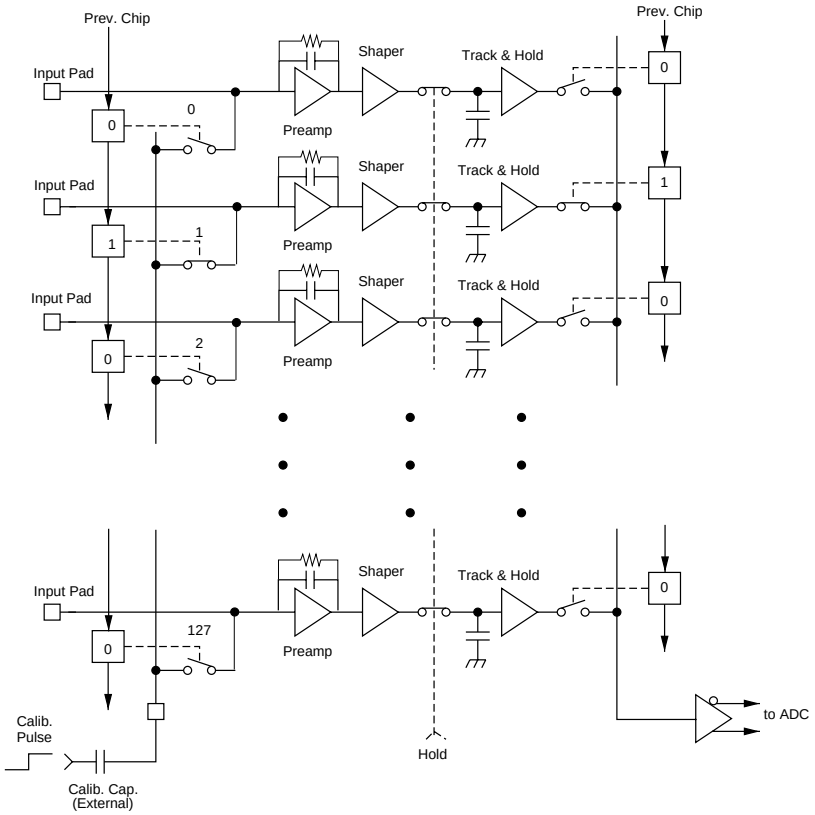


Figure 3.5: Block diagram of the VA1 chip

Figure 3.5 shows the block diagram of the VA1 chip. Signals from the strips are amplified by a charge sensitive amplifier, followed by a CR-RC shaper and sample

and hold circuit. When an external trigger causes the HOLD states to be asserted, the analog information from all channels is captured on storage capacitors and then sequentially read out using on-chip scanning analog multiplexers. The multiplexers from the five chips on a single hybrid are daisy chained and routed to FADCs, located in the electronics hut about 30 m away from the detector. Operation of the multiplexer is controlled by a shift register having one bit per channel. Figure 3.6 shows the readout sequence of the VA1 chip.

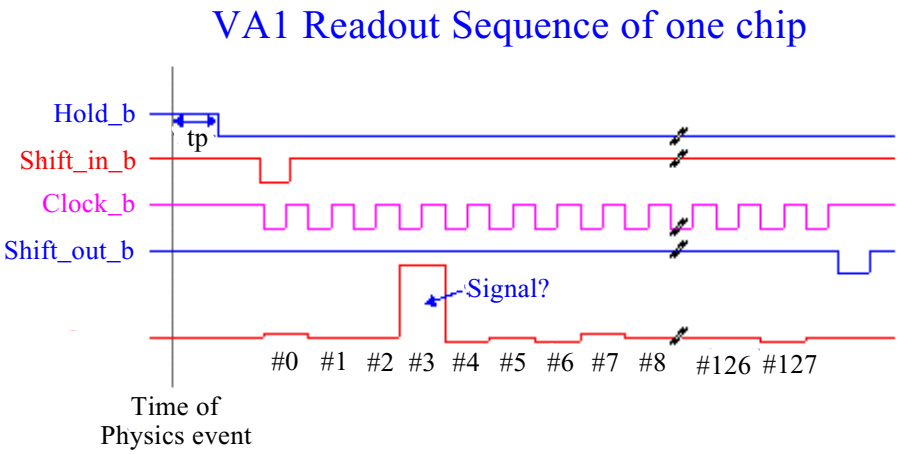


Figure 3.6: Readout sequence of the VA1 chip.

Although input-FET noise considerations of the VA1 propose a somewhat longer shaping time, the shaping time for the VA1s is adjusted to 1 μs to minimize the occupancy due to the beam background. Since the TOF can provide a fast trigger signal with approximately a 0.85 μs delay, which is shorter than the nominal Belle trigger system (called Level-1 trigger) latency (2.2 μs), a pretrigger signal from the TOF system (called Level-0 trigger for the SVD) is used to assert the VA1 HOLD line until the Level-1 signal is formed. If a Level-1 signal does not occur within 1.2 μs, the HOLD line is deasserted and the system is immediately ready for another event. If the Level-1 does occur, a normal readout sequence ensues. Figure 3.7 shows the operation sequence of the VA1. Note that the VA1 does not have a self-trigger function. Therefore, an external trigger information is needed to generate the HOLD signal.

CORE (COntrol and REpeater) System The repeater system [17] consists of small cards near the detector (ABCs), boards for signal buffering and front-end

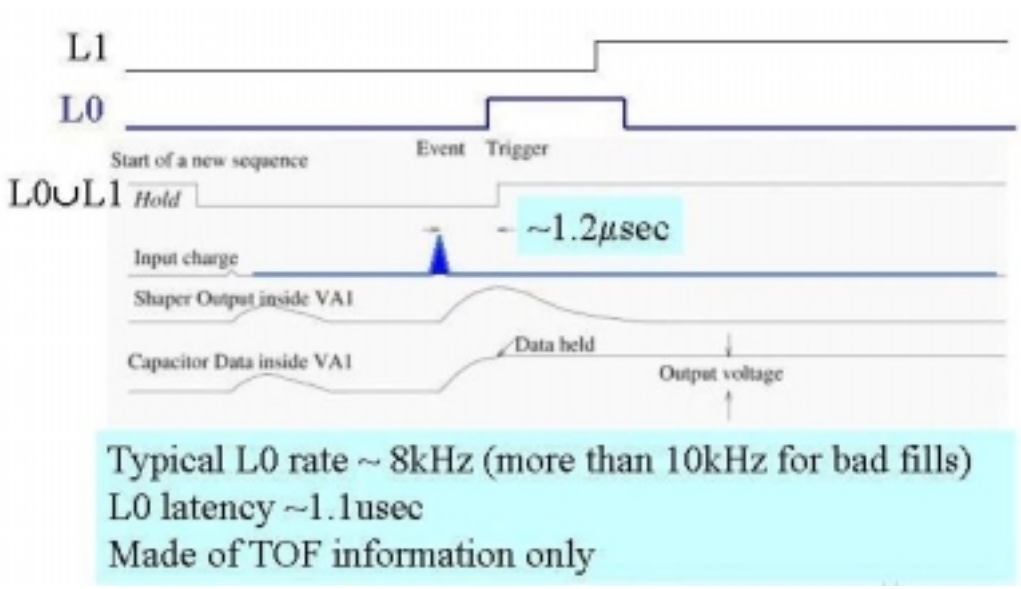


Figure 3.7: Operation sequence of the VA1 chip

control (REBO), a board for monitoring (RAMBO), a mother board (MAMBO) and their cooling shielding case (DOCK).

Signals from one side of DSSD are read by five VA1 chips on the hybrid board and sent to the repeater system through special 30 wires thin cables, which were provided by Omnetix Co. Ltd, USA. Two cables from two hybrid boards are merged on an ABC with 50 wires flat cable. The flat cable is connected to a MAMBO contained in a DOCK. A MAMBO has five slots. A RAMBO occupies the center slot, and four REBOs use the other slots.

Signals from the ABC are sent to the REBO through a local bus. After amplification and filtering, differential signals are sent to the back-end electronics system located in the electronics hut. A thermistor is mounted on each hybrid board to monitor the temperature of the front-end electronics. Voltage on a thermistor is read out by the RAMBO. All the timing and control signals, bias voltages and power supplies from backward electronics are fed to MAMBO and then distributed to each board or sent to front-end electronics.

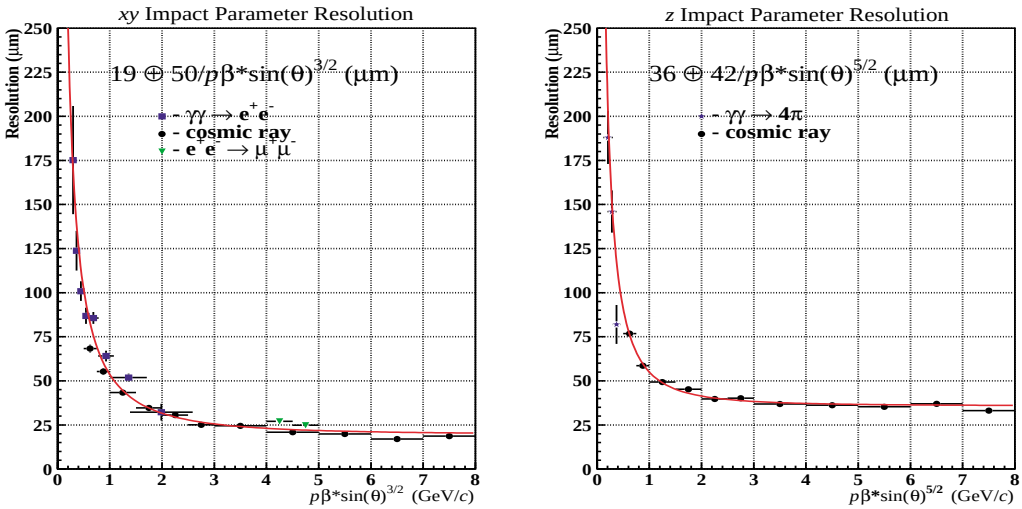
Since a DOCK can control and read out eight ABCs (or 16 hybrids), we have 8 DOCKs in total.

3.2.1.3 Performance

The impact parameter resolutions in the plane perpendicular to the beam axis and along the beam direction are measured [18] as Fig. 3.8 (a) and (b), respectively, and well represented by the following formula,

$$\sigma_{r\phi}^2 = (19)^2 + \left(\frac{50}{p\beta\sin^{3/2}\theta}\right)^2 \mu\mathrm{m}^2, \quad \sigma_z^2 = (36)^2 + \left(\frac{42}{p\beta\sin^{5/2}\theta}\right)^2, \mu\mathrm{m}^2 \tag{3.1}$$

respectively, where p is the momentum measured in GeV/c and β is the velocity divided by c.



(a) r-ϕ direction

(b) z direction

Figure 3.8: Impact parameter resolution.

3.2.2 Central Drift Chamber (CDC)

The main role of the Central Drift Chamber (CDC) is the detection of charged particles. Specifically, the physics goals of the Belle experiment require a momentum resolution better than $\sigma_{p_t}/p_t \sim 0.5 \cdot \sqrt{1+p_t^2}$ % for all charged particles with $p_t \geq$ 100 MeV/c. In addition, the CDC is expected to provide particle identification information in the form of precise dE/dx measurement for charged particles.

The structure of the CDC is shown in Fig. 3.9. The CDC covers $17° \leq \theta \leq 150°$, providing angular acceptance of 92 % of 4π in the $\Upsilon(4S)$ rest frame. The inner and outer radii are 8 cm and 88 cm, respectively. The CDC consists of 50 sense wire layers and 3 cathode strip layers. The sense-wire layers are grouped into 11 superlayers, where 6 of them are axial and 5 are stereo superlayers. The number of the readout channels is 8,400 for anode wires and 1,792 for cathode strips. 50 % Helium - 50 % ethane (C_6H_6) gas mixture is filled in the chamber to minimize the multiple-Coulomb scattering. A magnetic field of 1.5 Tesla is chosen to minimize momentum resolution without sacrificing efficiency for low momentum tracks.

The measured overall spatial resolution is 130 μm and the measured transverse momentum resolution is $(\sigma_{p_t}/p_t)^2 = (0.0019p_t)^2 + (0.0034)^2$. The dE/dx measurements have a resolution for hadron tracks of $\sigma(dE/dx) = 6.9\%$ and are useful for 3σ K/π separation below 0.8 GeV. The CDC also is useful for 4σ e/π separation. e/π separation below 1 GeV/c is very important for electron identification because the e/π method using the ECL is not effective in this momentum region.

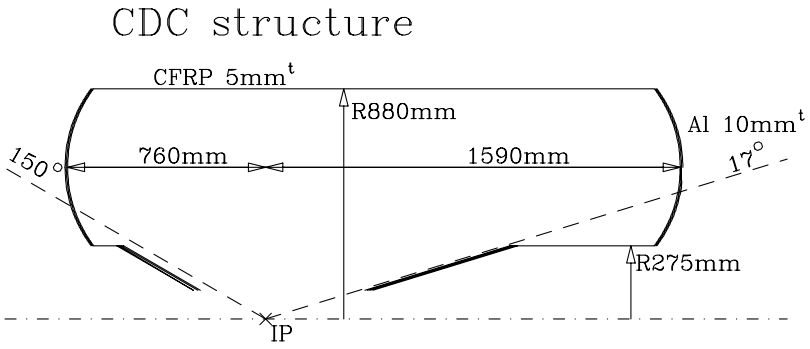


Figure 3.9: Structure of the Central Drift Chamber

The CDC trigger system uses signals from axial superlayers for the r-ϕ trigger. The z trigger is formed from the direct z information provided by the cathode strips and z coordinates inferred from the axial and stereo superlayers.

3.2.3 Aerogel Čerenkov counter (ACC)

The Aerogel Čerenkov counter (ACC) system extends the coverage for particle identification with the momentum $p \geq 1.2$ GeV/c, the upper limit of the Time of Flight system, from the kinematic limit of 2-body B decays such as $B^0 \to \pi^+\pi^-$, to $p = 2.5 \sim 3.5$ GeV, depending on the polar angle.

The configuration of the ACC is shown in Fig. 3.10. The aerogel of the ACC is made of SiO_2. The refractive index of the aerogel is chosen so that the pion produces Čerenkov light in the aerogel while the kaon does not. In general, the threshold of the Čerenkov light emission in a matter with the refractive index of n is represented using the velocity of particle β as follows:

$$n > 1/\beta = \sqrt{1 + (m/p)^2}, \tag{3.2}$$

where the particle momentum p is measured by the CDC.

Each aerogel counter module consists of silica aerogel radiator module and fine-mesh photo multiplier tubes to detect Čerenkov radiation. The typical aerogel module comprises aerogel tiles contained in a 0.2-mm-thick aluminum box.

The ACC is divided into two parts. A barrel array (BACC) covers an angular range of $34^\circ < \theta < 127^\circ$ and a forward end-cap array (EACC) covers an angular range of $17^\circ < \theta < 34^\circ$.

The BACC provides 3σ K/π separation in the momentum region 1.0 GeV $< p_K <$ 3.6 GeV. The BACC consists of 960 aerogel counter modules. Five different indices of refraction, n = 1.01, 1.013, 1.015, 1.020 and 1.028 are used depending on the polar angle. Each barrel counter is viewed by one or two fine-mesh photomultiplier tubes (FM-PMTs).

The EACC consists of 288 modules of which the refraction index equals to 1.03. This eliminates the need for the TOF system in end-cap region, since this refraction index gives $3\sigma K/\pi$ separation in the momentum range from 0.7 GeV/$c$to 2.4 GeV/c. This approach provides complete endcap flavor tagging, as well as particle identification for many of the few-body decays relevant to the CP eigenstates.

3.2.4 Time/Trigger of Flight Counter (TOF)

The relation between the measured flight time T and the particle momentum p measured by the CDC is as follows:

$$T = \frac{L}{c}\sqrt{1 + (m/p)^2}, \tag{3.3}$$

where L is the flight length and m is the particle mass. Because of the mass difference between kaons and pions, the difference of T between kaons and pions is $\sim$ 300 ps. The Time/Trigger of Flight Counter (TOF) has a time resolution of 95 ps and provides 3σ K/π separation. The TOF counters can provide fast timing signals for the trigger system with approximately a 0.85 μs delay.

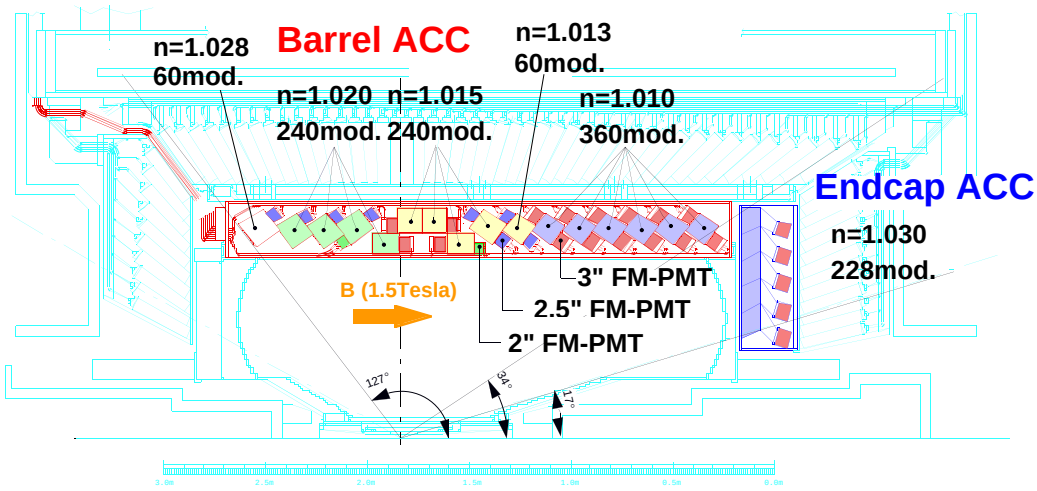


Figure 3.10: Configuration of the ACC

The TOF system comprises 64 barrel TOF/Trigger Scintillation Counter (TSC) modules. A TOF/TSC module consists of two trapezoid shaped 4-cm-thick counters and one 5-mm-thick TSC counter separated by a 2-cm gap as shown in Fig. 3.11. A coincidence between TSC and TOF counters rejects γ background and provides a clean event timing to the Belle trigger system.

The TOF is segmented into 128 in ϕ sectors and readout by one FM-PMT at each end. The TSCs have 64-fold segmentation and are readout from only the backward end by a single FM-PMT. The number of readout channels is 256 for the TOF and 64 for the TSC. Each module is located at $r = 120$ cm. The TOF/TSC system covers an angle range of $34° < \theta < 121°$.

3.2.5 Electromagnetic calorimeter (ECL)

The main purpose of the electromagnetic calorimeter (ECL) is the detection of photons from B meson decays with high efficiency and good resolution. Most of the physics goals of the Belle experiment require reconstruction of exclusive B meson final states. For typical B meson decays approximately one third of the final state particles are π^0's, thus it is important to have detection capabilities for photons that match those for charged particles, especially for low energy photon. π^0 mass resolu-

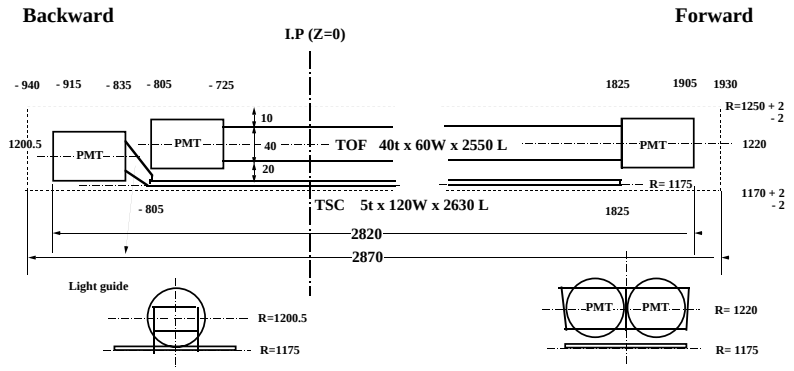


Figure 3.11: Configuration of TOF/TSC

tion is dominated by the photon energy resolution. Sensitivity to and resolution of low energy photons are the critical parameters for the efficient π^0 detection.

Electron identification in the Belle experiment relies primarily in comparison to the charged particle track momentum and the energy it deposits in the electromagnetic calorimeter. Good energy resolution of the calorimeter results in a better hadron rejection.

In order to satisfy these requirements, we chose a design of the electromagnetic calorimeter based on the CsI(Tℓ) crystal. All the CsI(Tℓ) crystals are 30 cm (16.1 radiation length) long, and are assembled into a tower structure pointing near the interaction point. The barrel part of the ECL has 46-fold segmentation in θ and 144-fold segmentation in ϕ.

The forward(backward) endcap part of the ECL has 13-(10-)fold segmentation in θ and the ϕ segmentation varies from 48 to 144 (64 to 144). The barrel part has 6,624 crystals and the forward(backward) endcap part has 1,153(960) crystals. Each crystal is readout by two 10 mm$\times$20 mm photo-diodes. The total number of the readout channel is 17,472. The inner radius of the barrel part is 125 cm. The forward(backward) endcap part starts at z=+196 cm($-$102 cm). The overall configuration of the ECL is shown in Fig. 3.12.

The raw signals from each CsI counter are combined through the readout electronics to form an analog sum for the Belle trigger system.

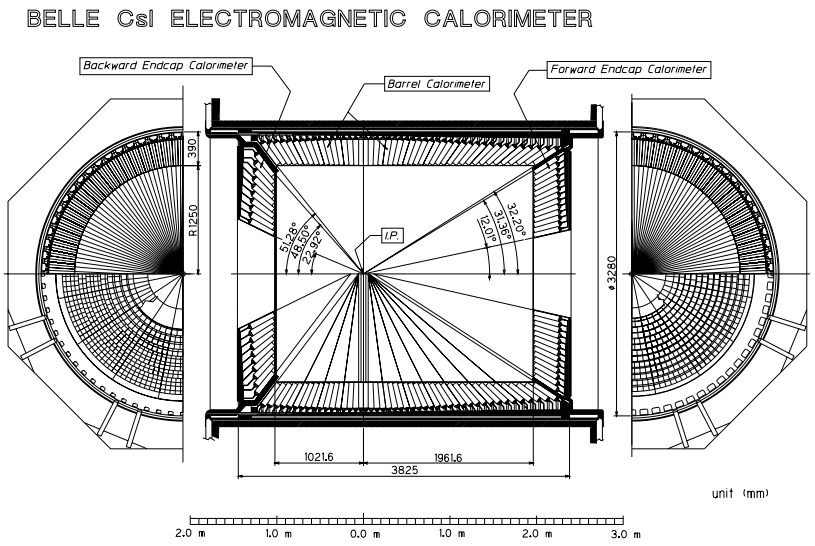


Figure 3.12: Configuration of the Electromagnetic Calorimeter

3.2.6 Solenoid magnet

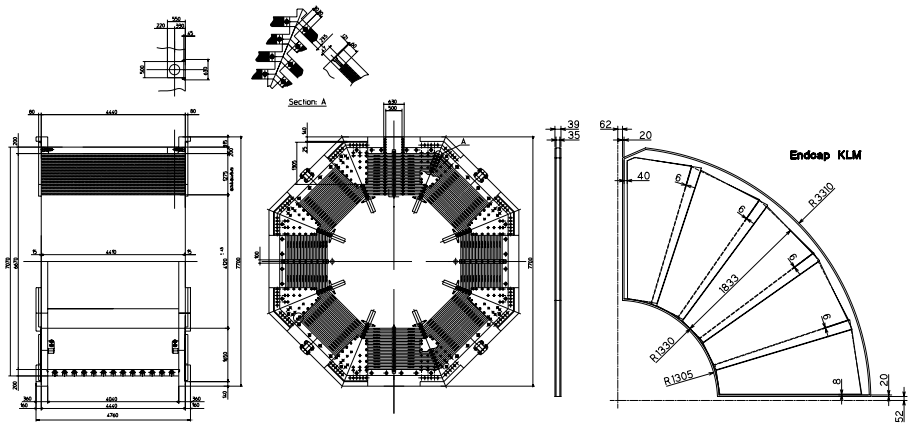
The magnetic field causes a charged particle to follow a helical path. Its curvature is related to its momentum. The coil consists of a single layer of an aluminum-stabilized superconductor coil, a niobium-titanium-copper alloy embedded in a high purity aluminum stabilizer. It is wound around the inner surface of an aluminum support cylinder. Indirect cooling is provided by liquid helium circulating through a single tube welded on the outer surface of the support structure. The super conducting solenoid magnet provides a magnetic field strength of 1.5 Tesla in a cylindrical volume of 3.4 m in diameter and 4.4 m in length. The field strength in the CDC volume is expected to vary by 2.0 %.

3.2.7 K_L and Muon Detector (KLM)

The KLM detects K_L and muon and measures their position. The detection of K_L is needed to reconstruct $B \to J/\psi K_L$. Muons are used in the CP violation measurements to identify the flavor of B mesons and to reconstruct $J/\psi \to \mu^+\mu^-$.

It consists of an octagonal barrel and two endcaps which are a sandwich structure of 14 iron plates of 4.4 cm thick and 14 (15 for barrel part) layers of 4.7 cm thick RPC (Resistive Plate Counter). The KLM system covers an angle range $25° < \theta < 145°$. In the case of K_L, the hadron shower occurs in its iron plates. However in the case

of muon, it does not occur. The barrel and endcap parts of the KLM are shown in Fig. 3.13.



(a) Barrel part (b) Endcap part

Figure 3.13: Barrel and endcap parts of the KLM

Raw output signals from each superlayer are sent to readout boards, located at the Belle detector, to discriminate noise signals and then barrel z and end-cap θ readouts are used for the triggering purpose.

3.2.8 Trigger System

The total cross sections and trigger rates at the luminosity of $10^{34}\text{cm}^{-2}\text{s}^{-1}$ for various physics processes of interest are listed in Table 3.1. We need to accumulate samples of Bhabha and $\gamma\gamma$ events to measure the luminosity and to calibrate the detector responses. However, since their rates are very large, these trigger rates must be prescaled by a factor $\simeq 100$. Because of their distinct signatures, this should not be difficult. Although the cross section for physics events of interest is reasonably small, they can be triggered in appropriately restrictive conditions.

The Belle trigger system consists of the Level-1 hardware trigger and the Level-3 software trigger. The latter has been designed to be implemented in the online computer farm. Figure 3.14 shows the schematic view of the Belle Level-1 trigger system. It consists of the sub-detector trigger systems and the central trigger system called the Global Decision Logic (GDL) [19]. The sub-detector trigger systems are

based on two categories: track triggers and energy triggers. The CDC and TOF are used to yield trigger signals for charged particles. The CDC provides r-ϕ and r-z track trigger signals. The ECL trigger system provides triggers based on the total energy deposit and cluster counting of crystal hits. These two categories allow sufficient redundancy. The KLM trigger gives additional information on muons and the EFC triggers are used for tagging two photon events as well as Bhabha events. The sub-detectors process event signals in parallel and provide trigger information to the GDL, where all information is combined to characterize the event type. Information from the SVD has not been implemented in the present trigger arrangement.

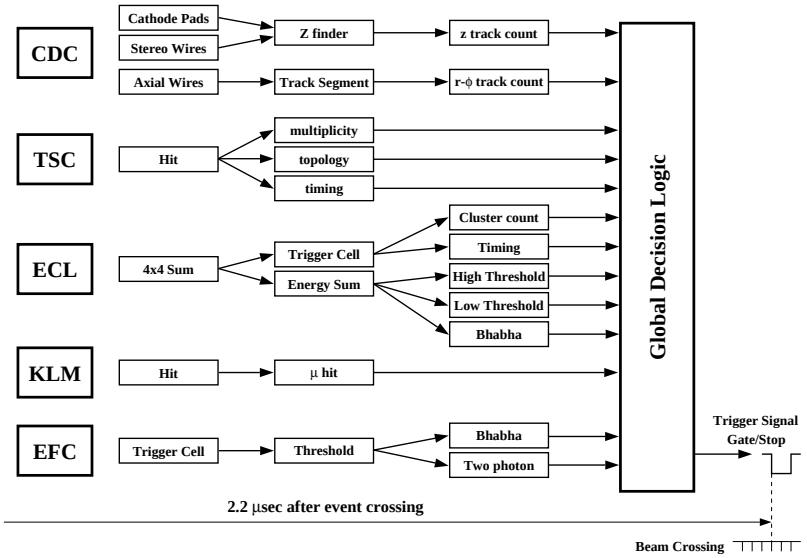


Figure 3.14: Belle trigger system

Considering the ultimate beam crossing rate of 509 MHz ($\sim$ 2 ns interval) with the full bucket operation of the KEKB, a "fast trigger and gate" scheme is adopted for the Belle trigger and data acquisition system. The trigger system provides the trigger signal with the fixed time of 2.2 μs after the event occurrence. The trigger signal is used for the gate signal of the ECL readout and the stop signal of the digital conversion for the CDC. Therefore, it is important to have good timing accuracy. The timing of the trigger is primarily determined by the TOF trigger which has the time jitter less than 10 ns. The ECL trigger signals are also used as timing signals for events in which the TOF trigger is not available. In order to maintain the 2.2 μs latency, each sub-detector trigger signal is required to be available at the GDL input by the maximum latency of 1.85 μs. Timing adjustments are done at the input of

the GDL. As a result, the GDL is left with the fixed 350 ns processing time to form the final trigger signal. In the case of the SVD readout the TOF trigger also provides the fast Level-0 trigger signal with a latency of ~ 0.85 μs. The Belle trigger system, including most of the sub-detector trigger systems, is operated in a pipelined manner with clocks synchronized to the KEKB accelerator RF signal. The base system clock is 16 MHz which is obtained by subdividing 509 MHz RF by 32. The higher frequency clocks, 32 MHz and 64 MHz, are also available for systems requiring fast processing.

Table 3.1: Total cross section and trigger rates with $L = 10^{34}\text{cm}^{-2}\text{s}^{-1}$ from various physics processes at Υ(4S). Superscript (a) indicates the values pre-scaled by a factor 1/100 and superscript (b) indicates the restricted condition of $p_t \geq 0.3$ GeV/c.

Physics process	Cross section (nb)	Rate (Hz)
$\Upsilon(4S) \to B\overline{B}$	1.2	12
Hadron production from continuum	2.8	28
$\mu^+\mu^- + \tau^+\tau^-$	1.6	16
Bhabha ($\theta_{lab} \geq 17^\circ$)	44	$4.4^{(a)}$
$\gamma\gamma$ ($\theta_{lab} \geq 17^\circ$)	2.4	$0.24^{(a)}$
2γ processes ($\theta_{lab} \geq 17^\circ$; $p_t \geq 0.2$ GeV)	~ 15	$\sim 35^{(b)}$
Total	~ 67	~ 96

3.2.8.1 CDC Trigger System

The CDC trigger is one of the key elements in the Belle trigger system. It is required to be fully efficient for charged tracks originating from the interaction point and relatively insensitive to background tracks from other sources. The CDC provides two type of triggers: the r-ϕ trigger based on signals from axial superlayers and the z-trigger which is formed from the direct z information provided by the cathode strips and z coordinates inferred from the axial and stereo superlayers.

r-ϕ trigger

The CDC r-ϕ trigger is the main component of the charged track trigger. It identifies tracks originating from the interaction point, discriminates against various background track sources, and makes a fast determination of the track p_t, the track di-

rection, and the number of tracks. The r-ϕ trigger is formed using discriminated axial-wire hit signals. Anode wires in each superlayer are grouped into track segment finder (TSF) cells and the hit pattern in each cell is examined by a memory look-up (MLU) table to test the presence of a candidate track segment. MLUs are latched periodically by a sample clock of 16 MHz.

Figure 3.15 shows the TSF cells for the CDC superlayers. The numbers of wires in a TSF cell are 17 for the innermost superlayer and 11 for outer superlayers, as shown Fig. 3.15 (a) and (b), respectively. In the order of the increasing superlayer radius, the numbers of TSF cells are 64, 96, 144, 192, 240, and 288.

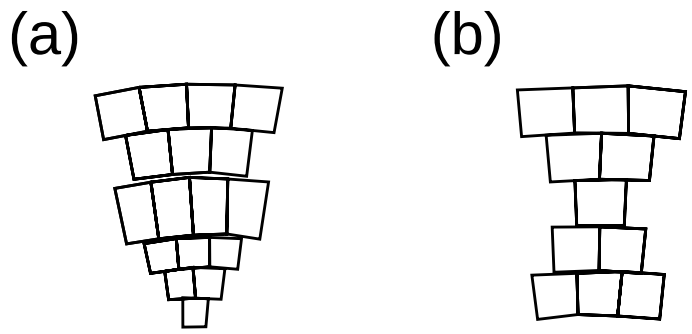


Figure 3.15: CDC track segment finder (TSF) cells for (a) innermost superlayer and (b) outer superlayers.

The TSF-cell outputs are logically OR'ed in a superlayer to form track finder (TF) wedges. Figure 3.16 shows one of 64 TF wedges. The number of TSF cells to be OR'ed depends on the chosen p_t threshold. The hit patterns of the TF wedges are fed into the next MLU stage. The second-stage MLU provides several output bits for different track categories according to patterns:

- short track (track in the three innermost trigger layers, $p_t \geq 200$ MeV/c) or
- full track (track which goes through all CDC trigger layers, $p_t \geq 300$ MeV/c).

The output signals from the 64 TF wedges are fed into the next stage to determine an event topology:

- counting of the number of short and full tracks,
- determination of the maximum opening angle between tracks, and

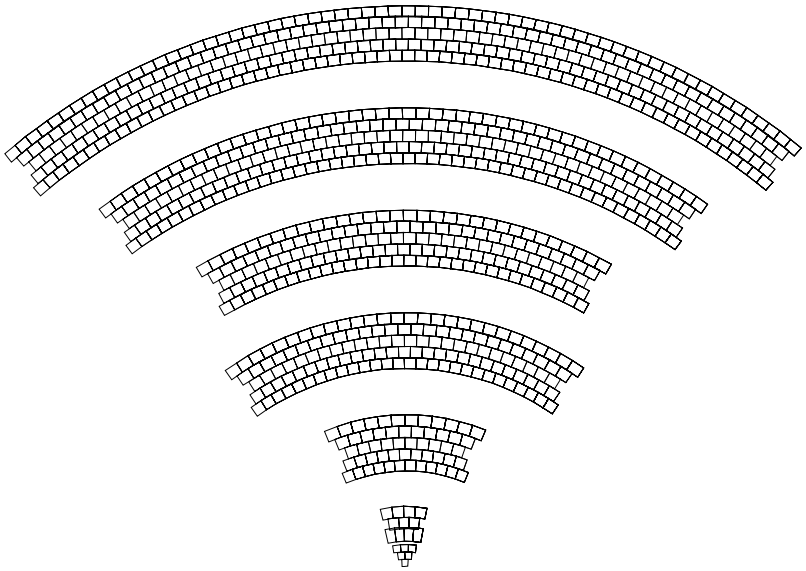


Figure 3.16: CDC track finder (TF) wedge.

- recognition of back-to-back track topologies.

The conditions are under software control and have considerable flexibility. The topology signals are sent to the GDL.

z trigger

The z trigger was designed to utilize the z-position information from the three cathode layers and the axial/stereo layers of the CDC. The cathode hit information provides direct information on the z-coordinate close to the interaction point. The accuracy of the cathode z-position is determined by the cathode-strip width of 8 mm and the cathode-strip-cluster size which is typically from 1 to 3 strips for a normally incident track. Since these cathode layers are located at the innermost CDC region, the additional z information provided by the stereo wires is necessary for good trigger performance. Figure 3.17 shows the hit distribution in each layer (called "trigger tower map"). One axial/stereo z-trigger layer consists of consecutive two axial and two stereo layers. Each pair of neighboring axial and stereo wires yields a calculated z-position. The coincidence of two axial or stereo layers is formed to reduce accidental trigger signals due to uncorrelated noise hits. The accuracy of calculated z-coordinates is around 50 mm for a single pair of axial stereo cell hits.

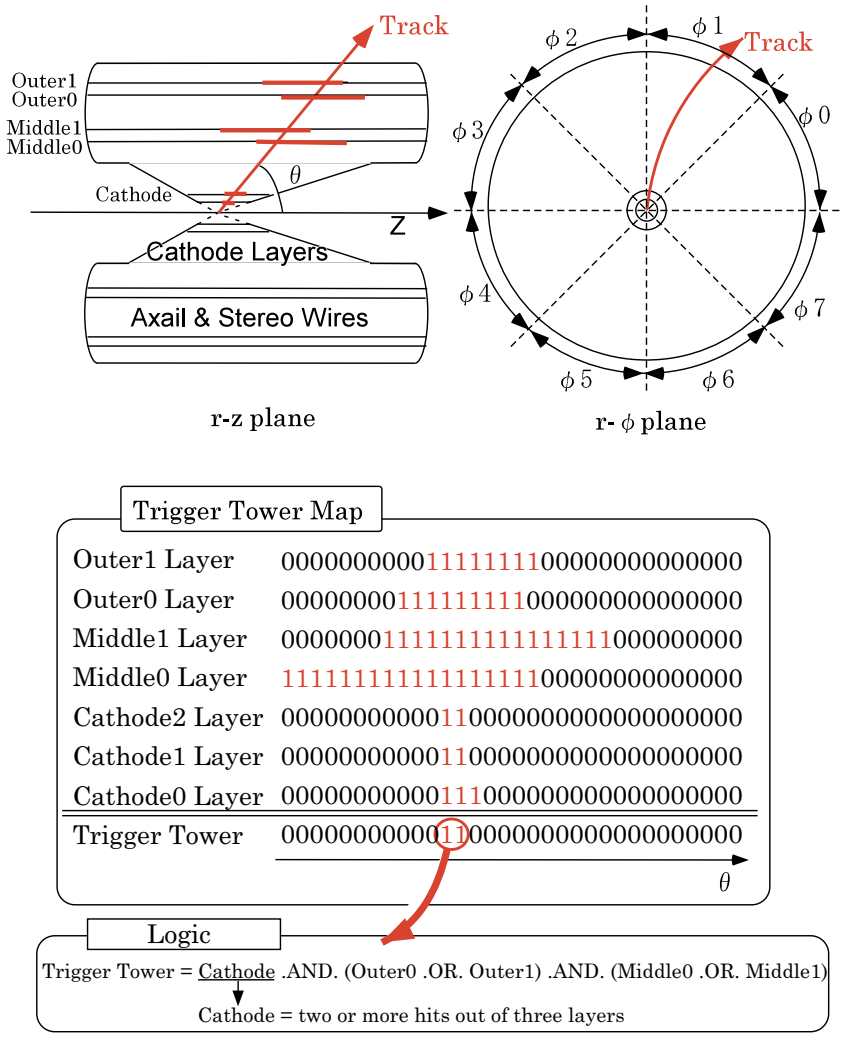


Figure 3.17: Hit distribution in each layer (trigger tower map). The z positions of each layer are calculated in 8 azimuthal segments individually. When a track passes through the CDC, as shown in the upper figure, it yields the trigger tower map shown in the lower figure.

The z-position is calculated in 8 azimuthal ϕ segments individually. In order to avoid the inefficiency for tracks around the ϕ segment boundary, the calculated z signals of adjacent ϕ segments are ORed. The tracks in the r-z plane (z-tracks) are reconstructed by seven sets of z-positions as shown in Fig. 3.17. A pattern yielded by tracks is represented by a "trigger tower map". When the z-positions in the inner and outer layers line up with the same tower bit, which presents the same polar angle from the z-axis (θ), it is regarded as being a track from the interaction point. In order to reduce the effects of inefficiencies of the CDC wire and cathode hits, we require at least two hit layers among the three cathode layers and at least one hit layer in each of the middle and outer layers with the logic shown in Fig. 3.17.

The schematic diagram of the z-trigger logic is shown in Fig. 3.18. There are five processes for the wire logic and four for the cathode logic. The number of the z-tracks formed by the trigger tower process is counted in the final decision process. Finally, a two-bit signal corresponding to the number of z-tracks originating from the interaction point is transmitted to the GDL.

Figure 3.19 shows the trigger efficiency as a function of the distance from the interaction point (dz) for single tracks with $p_t > 500$ MeV/c (left figure) and for events with the "at least one z-track" condition (right figure) for cosmic rays. The tracks originating from $|dz| > 10$ cm are effectively rejected. The efficiency is greater than 98 % for single tracks with $p_t > 300$ MeV/c.

In order to keep the efficiency high, we require at least one z-track in the actual trigger condition. Because of quite high hit rates at the innermost layers of the CDC due to the beam background, the rejection power of the z-trigger is reduced. Figure 3.20 shows the z distribution of the tracks for two-track events with and without the z-trigger requirement, in which we require at least one z-track. The z-trigger reduces about one-third of background events without losing beam interaction events.

3.2.9 TOF Trigger System

The TOF trigger system provides an event timing signal and information on the hit multiplicity and topology to the GDL. The multiplicity and topology information can be used to perform the internal event selection and reduce the rate of timing signals to acceptable levels before it is delivered to the GDL. A prompt Level-0 trigger signal is also delivered to the SVD based on independent event selection criteria.

The timing signal of an event is required to be sufficiently precise to make a gate

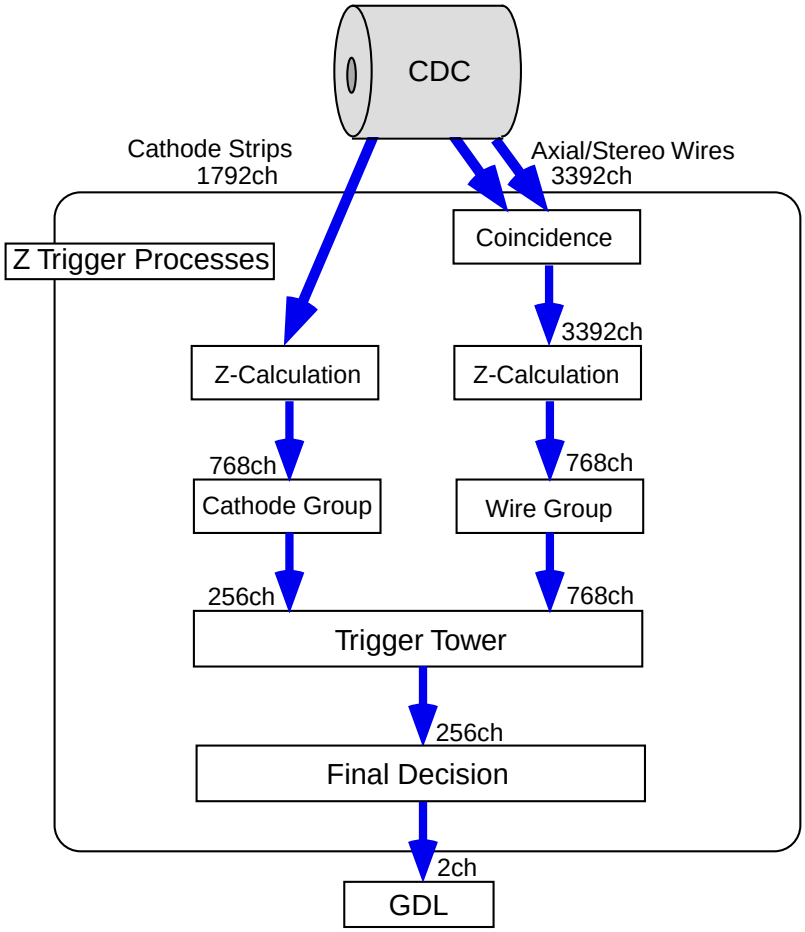


Figure 3.18: Schematic diagram of the z-trigger algorithm.

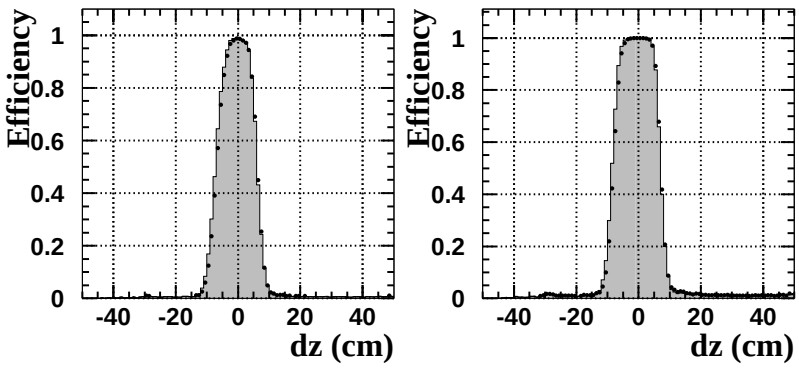


Figure 3.19: Relations between trigger efficiency and dz for a single track (left) and an event (right) with the "at least one z track" condition. The dots are the efficiency for cosmic ray data of the z-trigger logic, and the histogram is the efficiency for the reconstructed logic using CDC hit data as the input.

for the ECL readout and to provide a stop signal for the CDC readout, namely to have a time jitter less than 10 ns. Owing to the very fast time response of the TOF signals, a time jitter of about 5 ns is feasible. Although the timing of each PMT signal varies in a time range of $4 \sim 33$ ns depending on the hit position, the mean time stays within a small time range of $4.8 \sim 7.2$ ns for the Belle TOF configuration. The time jitter caused by variations in pulse height (time walk effect) is expected to be less than 1 ns at the nominal discrimination level. Thus, the TOF mean time can provide a precise event timing signal with a jitter of about 5 ns. This signal must be delivered at rates below 70 kHz to ensure only one timing signal to appear in the GDL event window.

The SVD readout electronics calls for a shaping time faster than ~ 2 μs required by the GDL to make an event decision. The TOF readout and trigger electronics can provide a prompt trigger signal with approximately a 0.85 μs delay. This includes ~ 500 ns to make internal event multiplicity levels. The trigger rate must be below 40 kHz to ensure a reasonable deadtime in the SVD readout electronics.

3.2.10 Data Acquisition System

The distributed-parallel system has been devised in the Belle data acquisition system. The global scheme of the system is shown in Fig. 3.21. The entire system is segmented into 7 subsystems running in parallel, each of them handling the data from sub-

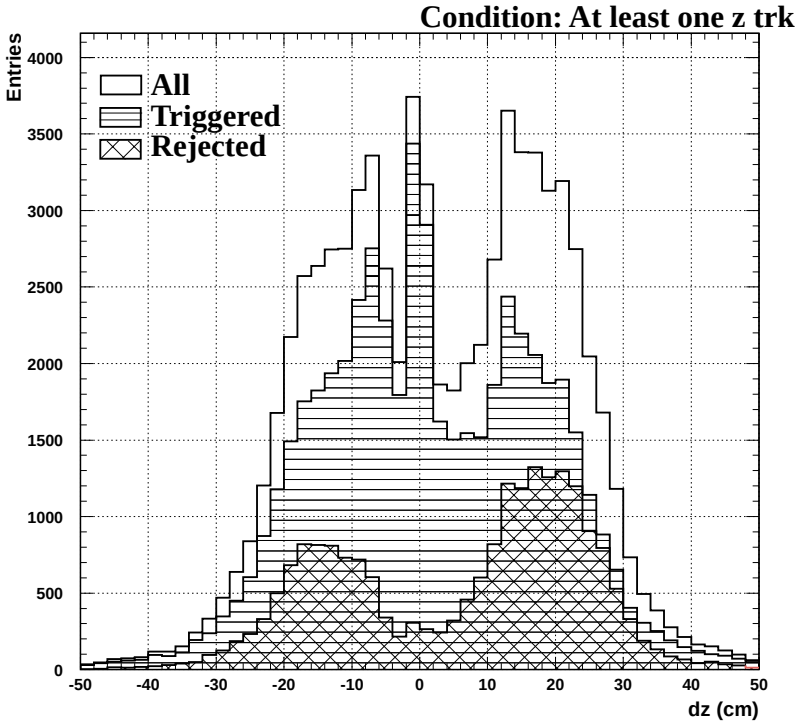


Figure 3.20: z distribution of two-track events with (single-hatched histogram) and without (blank histogram) z-trigger requirements. The cross-hatched histogram shows the z distribution of rejected events.

detector. Hit information on the sub-detectors is digitized in the different way from the SVD data acquisition. At the detector sub-system except for the KLM (and the SVD), the charge information on the sub-detectors is converted to time durations. We detect two edges of the durations. Timings of the edges with respect to a "common-stop" timing issued after the Level-0 trigger by a certain latency are digitized together with the hit signals from the KLM.

The final trigger asserted by the GDL is distributed to each detector sub-system (including the SVD) by the sequence controller. Receiving the final trigger, digitization by the TDC is started. While digitizing, the sequence controller blocks the next trigger. Digitization time, which is less than 200 μs, is the cause of the deadtime. This deadtime corresponds to the maximum trigger rate of 500 Hz. Digitized data from each subsystem are combined into a single event record by an event builder, which converts "detector-by-detector" parallel data streams to an "event-by-event" data river. The event builder output is transferred to an online computer farm, where

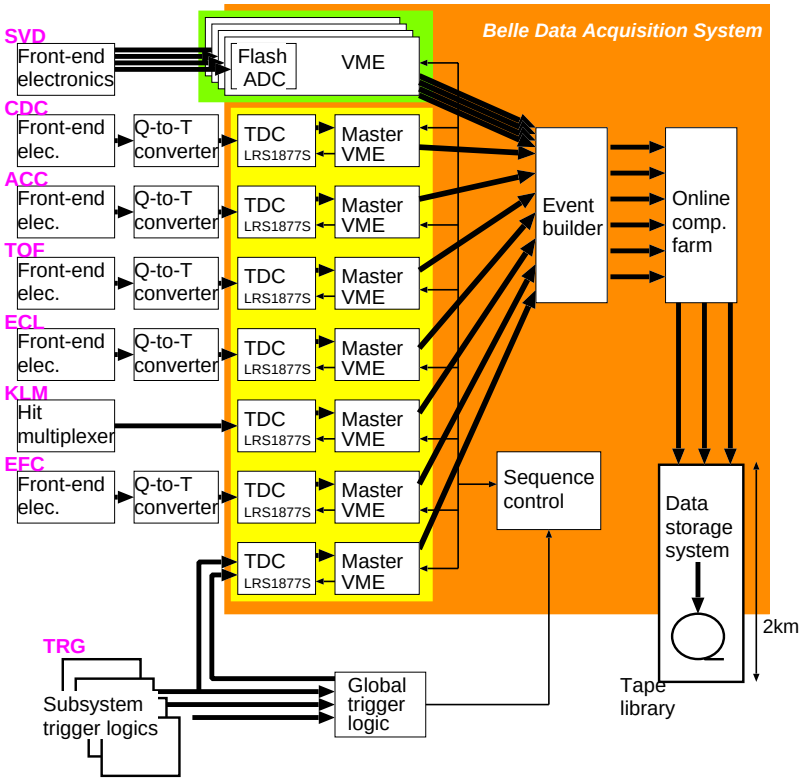


Figure 3.21: Belle DAQ system

another level of event filtering is done after fast event reconstruction (called as the "Level-3 trigger"). The data are then sent to a mass storage system located at the computer center via optical fibers.

Chapter 4

The Belle SVD Upgrade

As we described in Chapter 1, the better resolution and the trigger capability are required for the upgraded vertex detector. Therefore, we replace the present SVD (called SVD1, 3 silicon layers) and the inner layer of the CDC with a new expanded SVD (called SVD2, 4 silicon layers). The design of the SVD2 addresses the weak point of the SVD1. The SVD2 is expected to serve as the vertex detector for several years. When we add the 4th layer of the silicon ladder, we can reconstruct low momentum tracks with the SVD alone. This is beneficial to any mode that requires the detection of slow pions from D^*s.

Since the loss of z information from the inner cathode layer of the CDC causes reduction in trigger selectivity, the SVD2 is also needed to include trigger capability to offset that reduction.

In this chapter, we describe the new SVD2 design.

4.1 Limitations of SVD1

One of the most critical limitations of the SVD1 is its radiation tolerance. The radiation damage degrades the gain of the VA1, and it also increases the noise due to the leakage current of the DSSD.

Although the VA1 chip is tolerable against 200 kRad dose, it exhibits a significant increase in noise at lower levels. At the current luminosity, the SVD1 suffers from 100 kRad/year radiation. There is almost no margin for error in the accelerator and detector operations.

Limited angular acceptance is another weak point of the present SVD. It covers

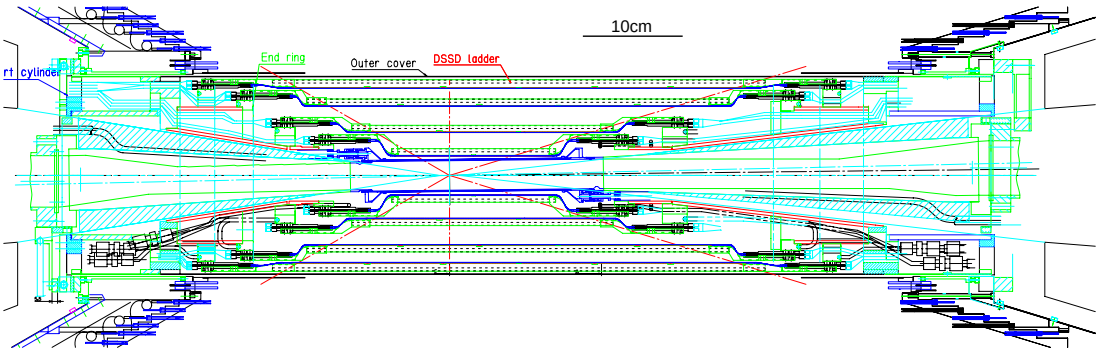


Figure 4.1: Side view of the SVD2

the polar angle range $23° < \theta < 139°$ while the CDC angular coverage is from $17° < \theta < 150°$. The effect of this reduced coverage is not limited to the loss of vertexing capability. Since the support material for the SVD ladder is in the tracking volume of the CDC, it degrades the performance of both charged particle tracking and neutral particle detection.

The relatively large radius of the innermost layer is another area ripe for improvement. The SVD1 uses a commercially available double-sided strip detector (DSSD), the S6936, which was originally developed for the DELPHI experiment at CERN. Due to the width of these DSSDs and the requirement of the overlap for alignment of the DSSDs, the minimum radius was 3 cm. To improve the impact parameter resolution, a smaller radius is highly desirable.

Despite these shortcomings, we believe that the basic design philosophy of the current detector — simplicity and reliance on the proven detector and readout IC designs — is correct and we seek to retain much of it.

4.2 Detector Configuration of SVD2

Taking into account the considerations above, we reached the following baseline design for the upgrade, SVD2. Figure 4.1 shows the side view of the SVD2.

The DSSD ladders form four layers concentrically with the beam pipe, as illustrated in Fig. 4.2. This figure shows the cross sectional view of the ladders at the interaction point (IP). Due to the added 4th layer, even if we only use the hit information from each layer of the SVD2 (more than 4 hits on the SVD), we can reconstruct low momentum tracks with errors. This is beneficial to any mode that requires the

detection of slow pions from D^*s. Table 4.1 summarizes the geometry of each layers.

The SVD2 consists of four layers of the DSSD ladders and covers the angular range $17° < \theta < 150°$. The innermost layer is located at a radius of $r = 2$ cm, while the outermost layer at $r = 8.8$ cm. All ladders in layer 1, 2, and 3 are constructed from identical DSSDs. The DSSDs are connected to the front-end ICs via a flex circuit. The front-end IC has a trigger capability and is tolerable against 20 MRad dose. The flex circuit also serves to fan out the signals from the z-strips, eliminating the need for a double-metal readout on the DSSD. Use of a flex circuit also allows the DSSDs to be placed closer to the interaction point, independent of support structure. The vertex resolution is improved to be from 200 μm to 150 μm with the closer innermost layer and added 4th layer [5]. Due to these configurations, the limitations of the SVD1 is overcome.

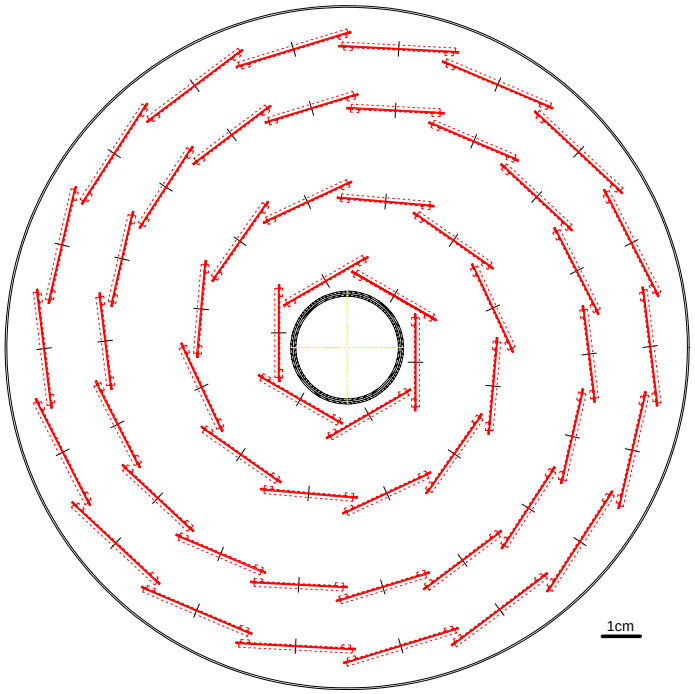


Figure 4.2: r-ϕ view of the SVD2

4.2.1 Mechanical Structure

The mechanical structure of the SVD2 consists of four layers of the DSSD ladders, end rings, support cylinders, and an outer cover as shown in Figs. 4.1 and 4.2. The

Table 4.1: Parameters of the SVD layers. The inner radius, number of DSSDs in ϕ, and number of DSSDs in z for each layer.

Layer	r (mm)	N_ϕ	N_z
1	20.0	6	2
2	43.5	12	3
3	70.0	18	5
4	88.0	18	6

forward and backward support cylinders are connected by the outer cover, and they form the basic mechanical structure of the SVD. The DSSD ladders are mounted on the forward and backward end rings, which are supported by the forward and the backward support cylinders. The support cylinders are in turn supported by the CDC structure. Since the precision of the machining and assembly is better than 50 μm, and the position of the DSSDs is measured with a precision of 10 μm for the SVD1, we expect the same precisions for the the SVD2. The beam pipe is also supported by the CDC structure. The beam pipe support is designed such that the heat load and any vibrations originating from the pipe and its cooling system should not affect the performance of the SVD system.

4.2.2 DSSD

Two types of the DSSDs (Double-sided Silicon Strip Detectors) are fabricated for the SVD2. We minimize the number of types of the DSSD to simplify bookkeeping and ladder assembly. In particular, in the layer 1, 2 and 3, the same sensors are used for all ladders.

The wider DSSDs are used in the outermost layer so that the total number of the ladders can be kept less than 30. This constraint comes from the available number of the readout channels in the repeater system. We chose 2.56×7.68 cm^2 and 3.33×7.38 cm^2 for the active DSSD size for the inner 3-layers (layer 1, 2, and 3) and the outermost layer, respectively. The length of the outermost DSSD is limited by the size of the silicon wafer (4 inches).

The DSSDs for the inner 3-layers consist of 512 ϕ-strips with 50 μm pitch and 1028 z-strips with 75 μm pitch. The DSSDs for the outermost layer consist of 512

ϕ-strips with 65 μm pitch and 1028 z-strips with 73 μm pitch. Every strip for the DSSDs in each layer is connected to a preamplifier channel. The flex circuits are used instead of double-metal structure to read out the z-strips to minimize the capacitance due to the overlap of readout traces and strips. Polysilicon resistors are implemented to bias each strip.

The ohmic side is used to measure the ϕ-coordinate while the junction side provides a z measurement. This arrangement allows us to balance the capacitance between the ohmic and junction sides. The p-stop structure is employed on the ohmic side to minimize the noise.

Tables 4.2, 4.3 and 4.4 summarize the specifications for the DSSD.

Table 4.2: Common specifications for all types of DSSDs

Parameter	Junction side	Ohmic side
Thickness	300 μm	
Readout(Bias) method	AC(Poly-Si)	
Full depletion voltage (V_{fd})	80 V Max	
Breakdown voltage	100 V Min	
Leakage current at V_{fd}	5 μA Max	
Bias resistance	10 MΩ typ.	
Passivation	SiO_2	

Table 4.3: Specifications for DSSD of the layer 1,2, and 3.

Parameter	Junction side	Ohmic side
Chip size	79.2 mm $\times$ 28.4 mm	
Active Area	76.8 $\times$ 25.6 mm	76.8 $\times$ 25.6 mm
Strip pitch	75 μm	50 μm
Number of strips	1024	512
Strip width	50 μm	12 μm
Readout electrode width	56 μm	10 μm

Table 4.4: Specifications for layer-4 DSSD.

Parameter	Junction side	Ohmic side
Chip size	76.4 mm × 34.9 mm	
Active Area	73.8 × 33.3 mm	73.8 × 33.3 mm
Strip pitch	73 μm	65 μm
Number of strips	1024	512
Strip width	55 μm	12 μm
Readout electrode width	61 μm	10 μm

4.2.3 Flex Circuits

In contrast to the SVD1, where the silicon sensors were wire-bonded directly to the VA1 readout chips, the SVD2 uses a flexible printed circuit board (flex) to connect the silicon sensors and the readout chips. The circuit is made on a film of the polyimide or the Kapton. The thickness of the film is about 25 μm. All the circuit lines and elements are on one side of the film with nothing on the other side. The trace material is copper. Two pads on the two ends of the lines are gold-plated and the rest covered by a mask to prevent oxidation. The thickness of the lines is about 5 μm .

4.3 Readout Electronics

Figure 4.3 shows a block diagram of the overall readout system. The readout system of the SVD2 is physically distributed over three sites: (i) VA1TA, the DSSD readout chips mounted on hybrids located in close proximity to the DSSDs; (ii) a COntrol and REpeater (CORE) system located about 2 m from the IP; and (iii) the FADC, DAQ, and trigger boards located in the electronics hut, which is an approximately 35 m cable run from the detector. The main upgrade is the implementation of the SVD trigger. We add the trigger capability to the readout chip VA1 and the ADC system. We call the readout chip, which consists of the VA1 part and trigger part (TA), as VA1TA. Four VA1TAs are mounted on one hybrid board. Figure 4.4 explains the data flow of the SVD2.

(1) Hit signals on the DSSDs reach the VA1TA chip. The signals are branched into the VA1 and the TA.

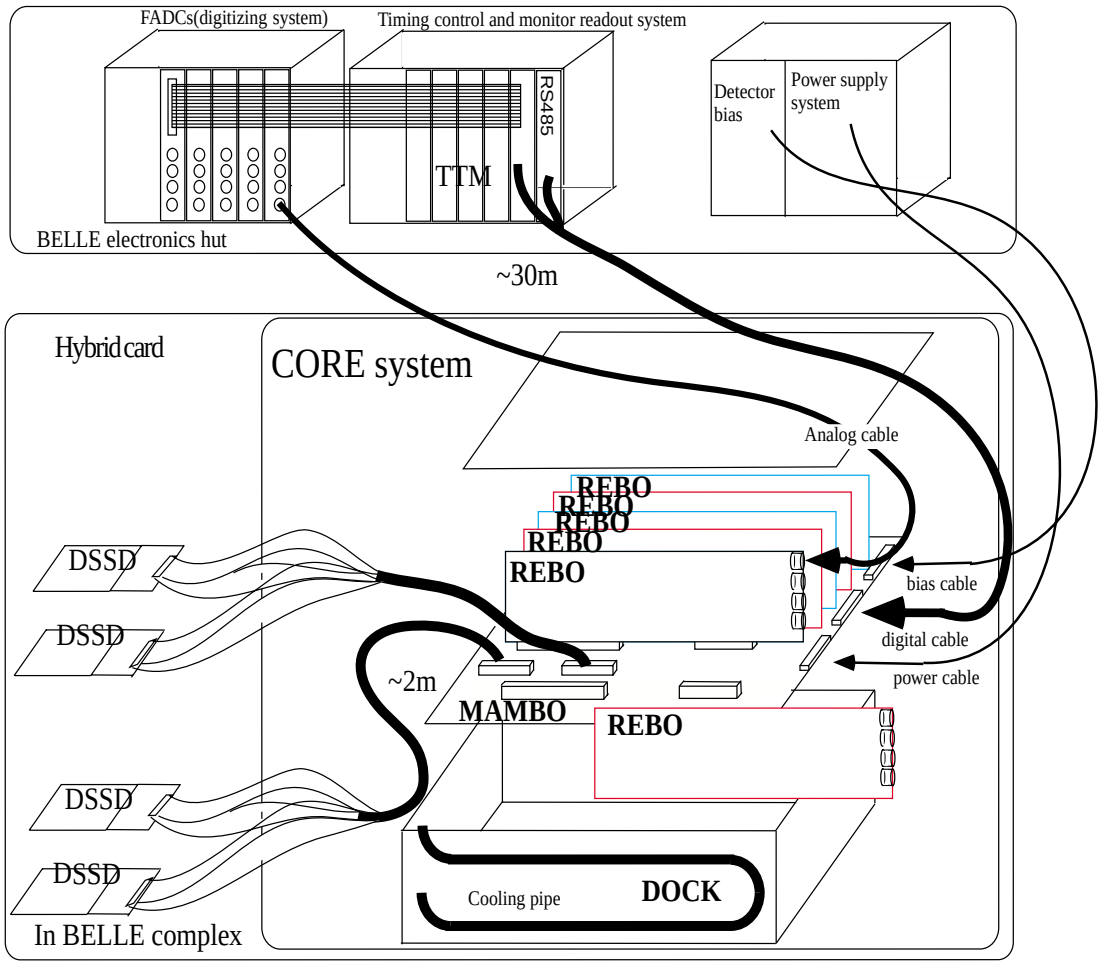


Figure 4.3: Block diagram of the SVD readout system

(2) The trigger signals from the TA enter the SVD trigger logic (L0T) via the ADCTF ("ADC with Trigger Facilities").

(3) The L0T combines the L0 signals from the TOF and the CDC with the TA output, and sends the combined signals to the GDL and the Trigger Timing Module (TTM). The TTM controls the VA1TA and the ADCTF upon the trigger.

(4) Upon the L0 trigger signal, the TTM sends HOLD signals to the VA1. When the VA1 receives the HOLD signals, the VA1 keeps the hit signals from the DSSDs.

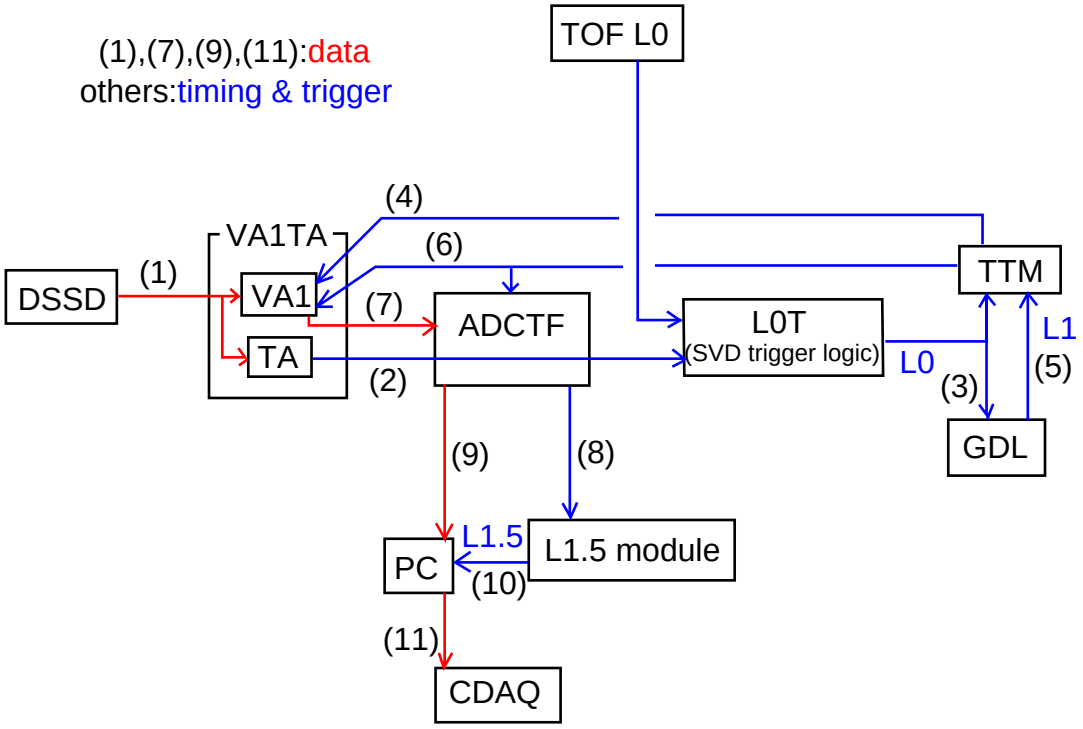


Figure 4.4: Block diagram of the SVD readout system. (1),(7),(9) and (11) signals are the data transfer. The others are timing and trigger signals. The detailed descriptions are noted in Sec. 4.3.

(5,6) The GDL sends L1 signals to the TTM so that the signal digitization is initiated. The TTM sends the clock and sampling timings to the VA1 and the ADCTF.

(7) The ADCTF invokes the data transfer from the VA1 to the ADCTF. The ADCTF digitizes the hit signals from the VA1s.

(8,9) The digitized data are transferred to the L1.5 module and PCs. The digitized data are processed (pedestal subtraction and zero suppression) on the PCs.

(10,11) The processed data are transferred to the central DAQ system via Ethernet when the L1.5 module asserts the trigger signal.

4.4 Trigger

The primary role of the present CDC cathode layers is to provide the L1 trigger signal. The CDC cathode z trigger has been providing the typical rate reduction of 0.8. The

axial layers in the cathode part are also used in the innermost Trigger Segment Finder (TSF) for the r-ϕ trigger. Thus the quality of the L1 r-ϕ track trigger will be also degraded. Using the data dedicated for beam background studies, it is estimated that we expect about 40 % increase in the trigger rate with the present logic, if we take out the innermost TSF.

Assuming that we have neither the CDC cathode nor the SVD trigger, the estimated Level-1 trigger rate at the design beam current can be about 1.2 kHz (0.1 kHz for physics process and 1.1 kHz for background) which is far beyond the limit of the bandwidth of the DAQ system (500 Hz) [5]. Although this estimation has rather large ambiguity, we should prepare this case and the rate reduction before the online computing farm (or in other words before the L3 trigger) is mandatory. It is apparently desirable for the SVD2 to have trigger capability at least to compensate for the loss by taking out the cathode part.

We are pursuing a two-pronged trigger strategy for the SVD2, consisting of a coarsely (segments of 128 strips) segmented system capable of providing prompt information as the Level-0 and Level-1 and a second system referred to at the Level-1.5, which makes use of finer information (segment of 16 $\sim$ 32 strips) extracted at the time of the serial scan of the VA1TA analog outputs (latency of 25 $\sim$ 50 μs).

4.4.1 Level-0 and Level-1 Triggers

The selectivity of both the Level-0 and Level-1 trigger must be improved if the Belle is to withstand the higher rates expected as the KEKB is upgraded. Reducing these rates will not only serve to reduce the deadtime, but will also lighten the load on the downstream DAQ and offline data processing systems.

Each of the VA1TAs generates one prompt trigger output by taking the OR of the 128 strip signals. Total 864 trigger signals (equals to the number of the VA1TAs) can be combined in the L0T both the r-ϕ and the r-z views in such a way as to do a simple tracking by the memory look up technique. Combining the VA1TA outputs with the current Level-0 trigger that is now based solely on a coincidence of the TOF counters will result in a significant reduction of the overall trigger rate. The newly installed small-cell inner layers of the CDC (SC CDC) can also be utilized in the L0T. Figure 4.5 shows the r-ϕ view of the SVD2 and the small-cell CDC.

Figure 4.6 shows a block diagram of the L0T. The L0T is the place where the signals from the VA1TA, the SC CDC and the TOF are merged. At the L0T, a trigger signal is generated and branched into two: one is routed to the VA1 via the

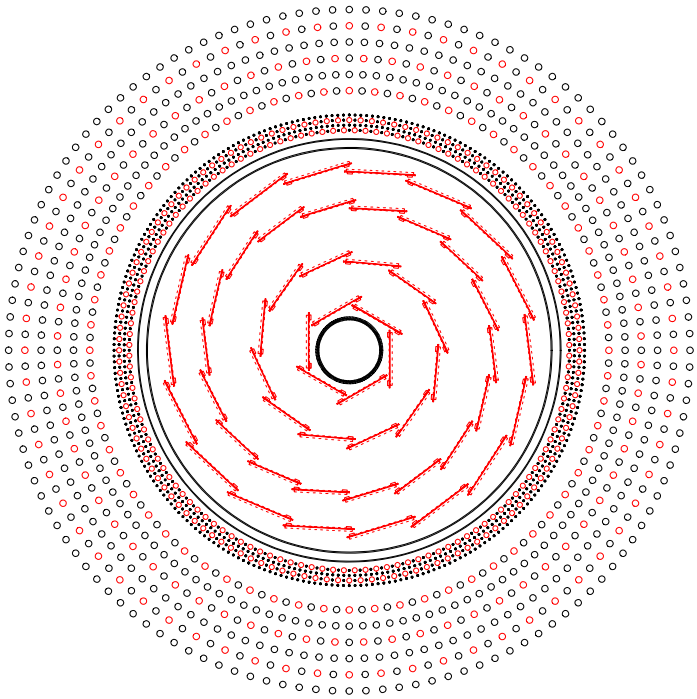


Figure 4.5: r-ϕ view of the SVD2 and the small cell CDC

TTM to hold the hit signals on the DSSDs, and the other is fed to the GDL where the L1 trigger is decided with the track and total energy information. According to the L1 trigger, all detector sub-systems start the signal digitization and the data taking procedure.

The TA is required to generate trigger signals 475 ns (Table 4.5) before the peaking time of the VA1. Since the optimized peaking time of the VA1 is 600 ns [20], the TA must assert the trigger signals in 125 ns after the DSSDs are hit.

Table 4.5: Latencies of each component other than the TA.

Sources	Latencies (ns)
Cable	300
ADCTF	50
L0T	100
TTM	25

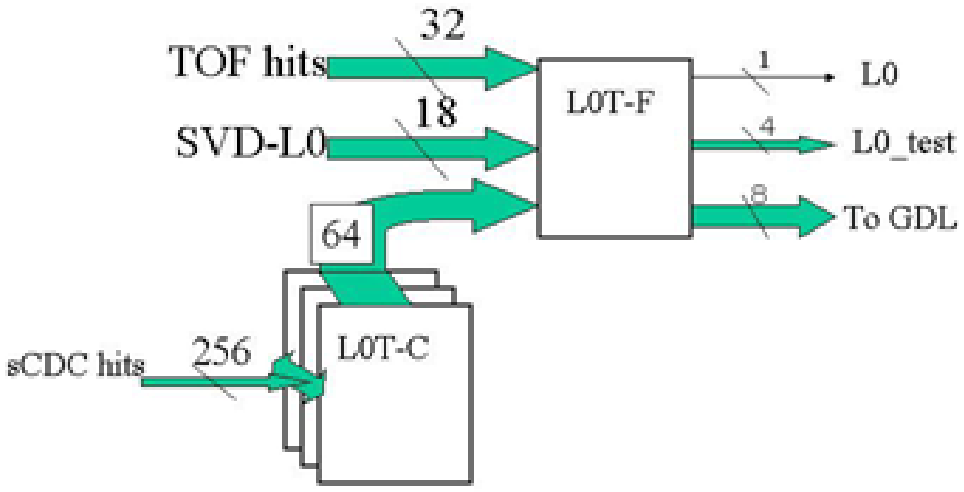


Figure 4.6: L0T system block diagram.

4.4.2 Level-1.5 Trigger

To lighten the load of the central DAQ system, we install the Level-1.5 trigger. The basic idea of the Level-1.5 trigger is to extract the trigger information during the scanning of the analog multiplexers of the VA1 chips.

The dominant source of the false triggers at the Level-1 is beam-gas interactions, of which tracks are not originated from the e^+e^- interaction points. Since the Level-1.5 trigger can provide the z position of the event vertex, it can reduce the beam-gas background more effectively than the Level-1 trigger.

Chapter 5

Performance of the VA1TA

We use the VA1TA chip which augments the VA1 with a parallel set of the fast shaping channels that are used to provide a prompt digital output for triggering. The VA1TA is essential for the trigger function of the SVD2. In this chapter, we describe the performance of the VA1TA chip.

5.1 VA1TA Design

5.1.1 Architecture of the VA1TA

The picture of the VA1TA chip is shown in Fig. 5.1. The VA1TA is a 128-channel preamplifier-shaper integrated circuit. Each channel has a preamplifier, a slow shaping time amplifier (slow shaper), a fast shaping time amplifier (fast shaper), a discriminator and a monostable multivibrator.

Figure 5.2 shows a schematic diagram of the VA1TA. Figure 5.3 shows signal, trigger and data sequences in the VA1TA. The output from the slow shaper corresponds to the analog output of the VA1 part ((a) in Fig. 5.3). The readout sequence of the VA1 part is the same as that of the original VA1 described in Sec. 3.2.1.2.

The TA part consists of the fast shaper, the discriminator, and the monostable multivibrator. There is also a high-pass filter (not shown in the figure, placed in front of the discriminator) with a very low cutoff frequency in order to reduce the offset-spread across the chip. The fast shaper uses the same preamplifier as the slow shaper. If the pulse height of the fast shaper output ((b) in Fig. 5.3) is larger than the threshold voltage of the discriminator, a trigger bit signal is asserted via the monostable mutivibrator ((c) in Fig. 5.3). The trigger signals from 128 channels are

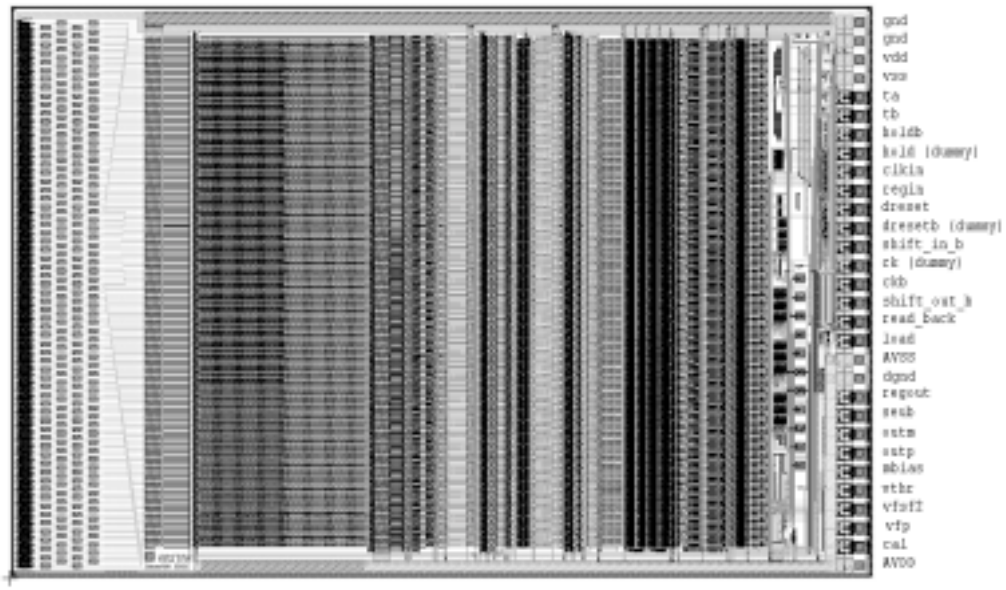


Figure 5.1: Picture of the VA1TA chip

wire-OR'ed (i.e. one trigger output per one chip).

The VA1TA provides testing inputs of the individual channels. The gain of the VA1TA can be calibrated by the test pulses.

The VA1TA is fabricated with the AMS 0.35 μm process. It is known that the radiation hardness scales as the cube of process in deep sub-micron region. The VA1 with the AMS 0.35 μm process is measured for the radiation hardness to be over 20 MRad [21].

5.1.2 Control Parameters

We have some parameters to control the function of the VA1TA, such as the threshold of the discriminator and the feedback resistance of the shapers. These parameters are controlled by the on-chip DACs. The on-chip DAC values are set externally using a 680-bit long shift register.

The parameter "Pre_bias" controls the bias current for the preamplifier. The MOS-FETs are used as the feedback resistances of the preamplifier and the shapers.

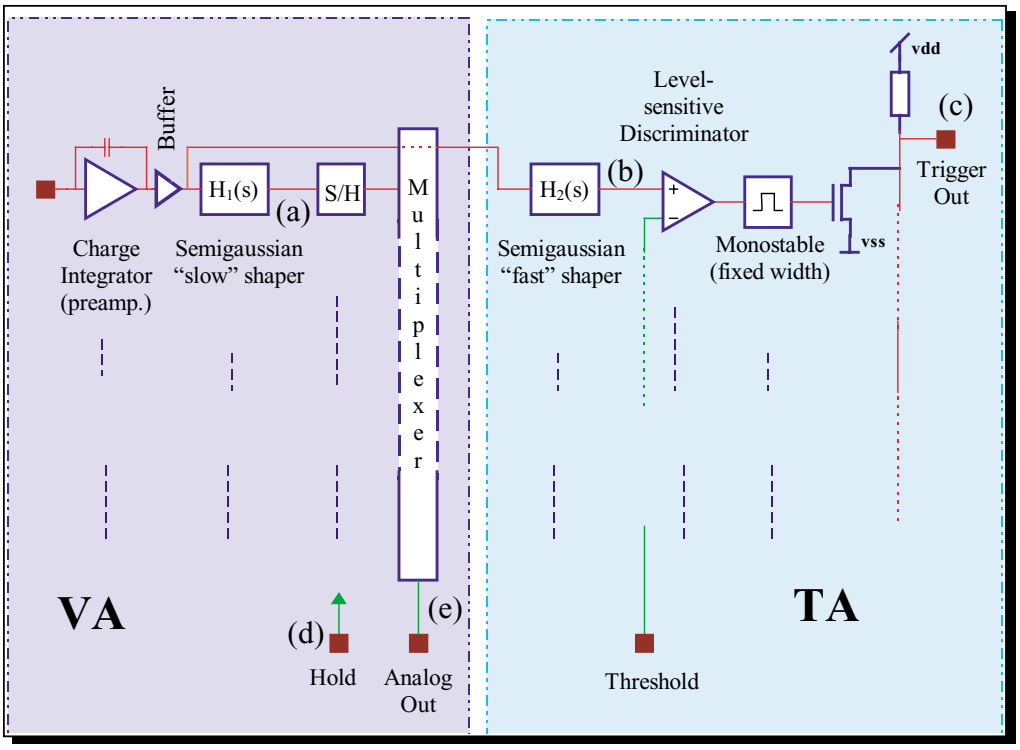


Figure 5.2: Schematic view of the VA1TA principle

The DC current for the preamplifier feedback resistance is changed by the "Ifp". The "sbi" and "Ifsf" ("Sha_bias" and "Ifss") control the bias current and the feedback resistance of the fast (slow) shaper, respectively. The peaking time of the slow shaper can be changed from 0.3 μs to 1.0 μs. For the fast shaper, we can choose the nominal peaking time to be 75 ns or 300 ns using the "Tp300". We can tune the peaking time changing the "sbi" and "Ifsf" parameters.

We can set the threshold of discriminators using the on-chip DAC, "Vthr". Table 5.1 shows the relation among the DAC value, the nominal threshold, and the measured positive and negative threshold voltages. The nominal threshold value for each DAC setting is shown in terms of the equivalent input charge of the preamplifier. Since the gains of the preamplifier and the fast shaper are different channel-by-channel, the threshold value are different channel-by-channel. Each channel includes a four bit DAC to trim the threshold voltage channel-by-channel. The threshold dispersion is required to be from 200 e^- to 400 e^-. The "obi" controls the bias current for the

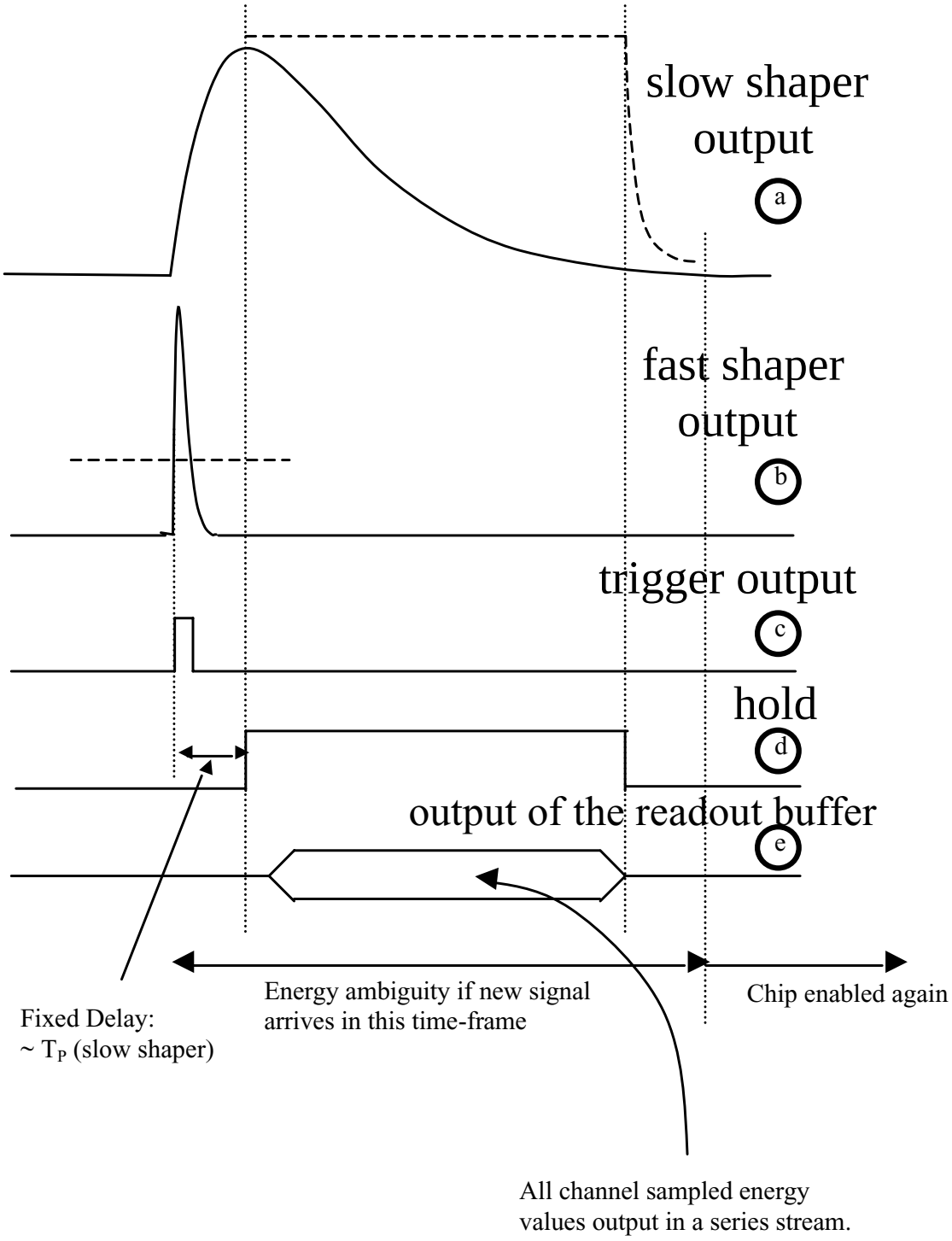


Figure 5.3: Signal, trigger and data sequences in the VA1TA

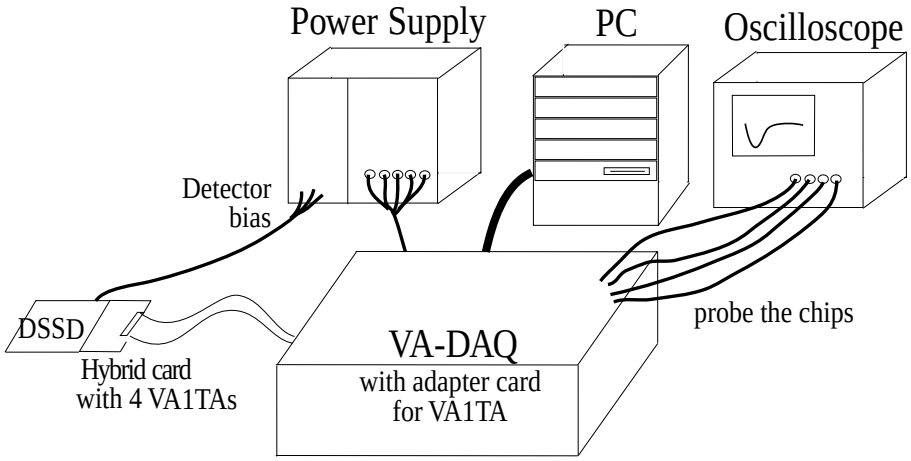


Figure 5.4: Test environment for the VA1TA. We can test the VA1TA with or without the DSSD using the VA-DAQ. The PC controls the VA-DAQ. We probe signals on the VA-DAQ.

discriminator. The bias current for the high-pass filter in front of the discriminator is changed by the "vrc".

Table 5.2 and Table 5.3 show the summary of the effects of the control parameters and basic specification of the VA1TA chip, respectively.

5.2 Test Environment

We use 'VA-DAQ' [22], which is provided by IDEAS, to operate the VA1TA chip. The VA-DAQ provides the bias voltage, the clock, the hold signal, the serial shift register mask, and the test pulse.

The VA-DAQ can read out both the analog and trigger outputs channel-by-channel. The VA-DAQ is fully controlled with a PC through the parallel port. All analog outputs from the VA1TA are digitized on the VA-DAQ and read out by the PC. The overall test environment is illustrated in Fig. 5.4. The picture of test sample is shown in Fig. 5.5. One of the four VA1TA chips is wire-bonded to the ohmic side (n-side) of the DSSD.

Table 5.1: Relations between the threshold DAC value, the nominal threshold, the measured positive and negative threshold voltage.

DAC Values	Nominal Threshold (Equivalent input charge)	Measured Positive Threshold (mV)	Measured Negative Threshold (mV)
0	2000 e^-	2.3	-8.5
1	2200 e^-	2.8	-9.0
2	2400 e^-	3.4	-9.5
3	2600 e^-	3.9	-10.0
4	2800 e^-	4.4	-10.6
5	3000 e^-	4.9	-11.1
6	3200 e^-	5.5	-11.7
7	3400 e^-	6.0	-12.2
8	3600 e^-	6.5	-12.7
9	3800 e^-	7.1	-13.2
10	4000 e^-	7.6	-13.7
11	4200 e^-	8.1	-14.2
12	4400 e^-	8.7	-14.8
13	4600 e^-	9.2	-15.3
14	4800 e^-	9.7	-15.9
15	5000 e^-	10.2	-16.3
16	5200 e^-	10.8	-17.0
17	5400 e^-	11.4	-17.5
18	5600 e^-	11.9	-18.0
19	5800 e^-	12.4	-18.4
20	6000 e^-	12.9	-19.1
21	6200 e^-	13.4	-19.6
22	6400 e^-	14.0	-20.1
23	6600 e^-	14.5	-20.6
24	6800 e^-	15.0	-21.2
25	7000 e^-	15.5	-21.7
26	7200 e^-	16.1	-22.2
27	7400 e^-	16.6	-22.7
28	7600 e^-	17.1	-23.3
29	7800 e^-	17.6	-23.8
30	8000 e^-	18.1	-24.3
31	8200 e^-	18.6	-24.8

Table 5.2: Effects of the control parameters.

Parameter	Effect
obi	The bias current for the discriminators.
Pre_bias	The bias current for the preamplifiers.
sbi	The bias current for the fast shapers.
vrc	The bias current for the high-pass filter in front of the discriminators.
Ifp	DC current for controlling the preamp feedback resistance (NMOS device).
Ifsf	DC current for controlling the fast shaper feedback resistance (NMOS device).
Ifss	DC current for controlling the slow shaper feedback resistance (NMOS device).
Sha_bias	The bias current for the slow shapers.
Tp300	The shaping time of the fast shaper.
Vthr	This voltage set the threshold of all the 128 discriminators on the chip.
channel trim DACs	This voltage tune the local (channel-by-channel) threshold.

Table 5.3: Basic specifications of the VA1TA.

Parameter	Value
Process technology	AMS 0.35 μm CMOS with epitaxial layer
Front-end	128 channels
Shaping time (slow)	0.3 μs $\sim$ 1.0 μs
Shaping time (fast)	75 or 300 ns
Threshold (discri.)	2000 $\sim$ 8200 e^- at 200 e^- step
Threshold dispersion	200 $\sim$ 400 e^-

Table 5.4: Fit results of the VA1 part noise. For comparison, the previous results are also shown.

Result	A (e^-)	B ($e^-\mu$s)
Measured result	0	211
Previous result	0	217

5.3 Performance of the VA1 Part

Since the VA1TA is a successor to the VA1, it is important to measure the VA1 part performance and to compare it with the previous result [23].

We measure the noise as a function of the shaping time of the slow shaper. The result is shown in Fig. 5.6. We expect that the noise is given by $ENC(T_p) = \sqrt{A^2 + B^2/T_p}$, where T_p, A, and B^2/T_p are the shaping time of the shaper, the flicker noise, and a series noise square (a quadratic sum of the channel noise and the bulk-resistance noise), respectively [15]. Table 5.4 shows the fit results together with the previous result. Our result is consistent with the previous one.

The VA1 part is further evaluated by connecting it to the ohmic side strips of the DSSD. Figure 5.7 shows the relation between the measured noise and the detector bias voltage. The detector seems fully depleted at 70 V and the noise is constant above the depletion voltage.

Noise characteristics with the DSSD are further studied by varying the shaping time. Figure 5.8 shows the noise values measured for the VA1TA sample connected to the DSSD. While the T_p dependence below $T_p = 0.7$ μs is similar to that in Fig. 5.6,

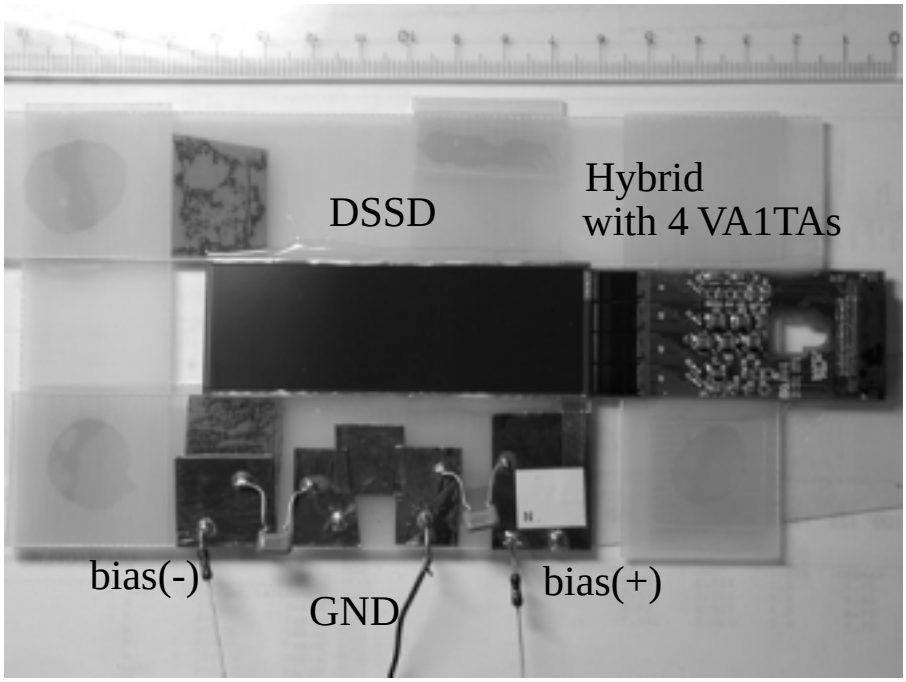


Figure 5.5: Picture of the test sample.

the thermal and shot noise from the DSSD increases the total noise above $T_p = 0.8$ μs. For the shaping time = 0.7 μs, the measured noise is 516 e^-. This corresponds to the S/N ratio of 36 and satisfies the requirement, S/N > 10.

We summarize the measured result with the shaping time = 0.7 μs in Table 5.5. For comparison, the previous results for the VA1, which was produced similarly with AMS 0.35 μm process, are also shown. Since the measured results are consistent with the previous results, the performance of the VA1 part is confirmed to be satisfactory.

Table 5.5: Measured noise of the VA1 part. For comparison, the previous results are also shown.

Result	$ENC(e^-)$ without DSSD	$ENC(e^-)$ with DSSD
Measured result	230	520
Previous result	200	520 (T_p=0.8 μs)

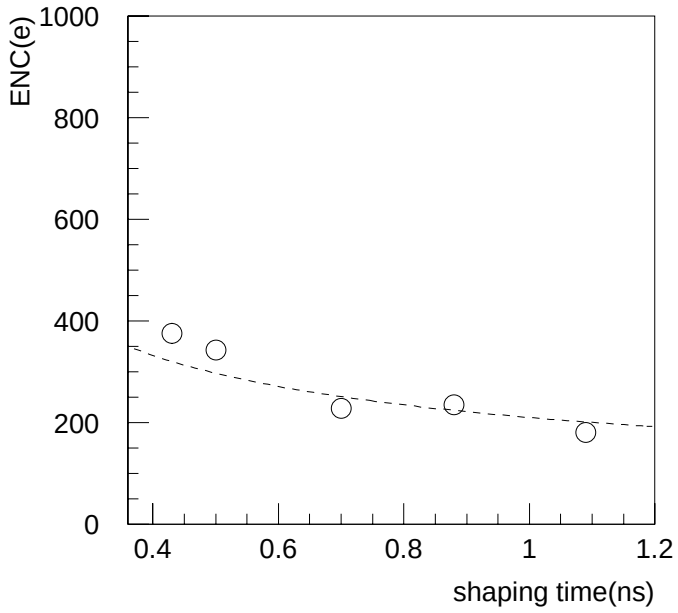


Figure 5.6: VA1 part noise as a function of the shaping time.

5.4 Performance of the TA Part

In this section, we check the performance of the TA part. Figure 5.9 shows the outputs from the VA1 part and the TA part. The lines (a), (b), and (c) are the test pulse, the analog output, and the trigger signal from the TA, respectively. In order to test the capability of the VA1TA to provide a fast trigger signal, we measure the lowest threshold, tuning parameter effect, trigger timing, and threshold dispersion of the VA1TA.

5.4.1 Threshold and Noise

We measure the threshold level and the noise of the TA part. As shown in Fig. 5.2, we cannot see the raw signal from the fast shaper directly. (We can only see the output of the discriminator, a trigger "bit".) However, we can estimate the threshold and the noise from the distribution of the fraction of the triggered events as a function of the input charge.

Figure 5.10 shows an example of the threshold measurement and fit result. The horizontal and vertical axes are the injected charge and the number of triggered events, respectively. In this measurement, we have injected the test pulse 200 times for each

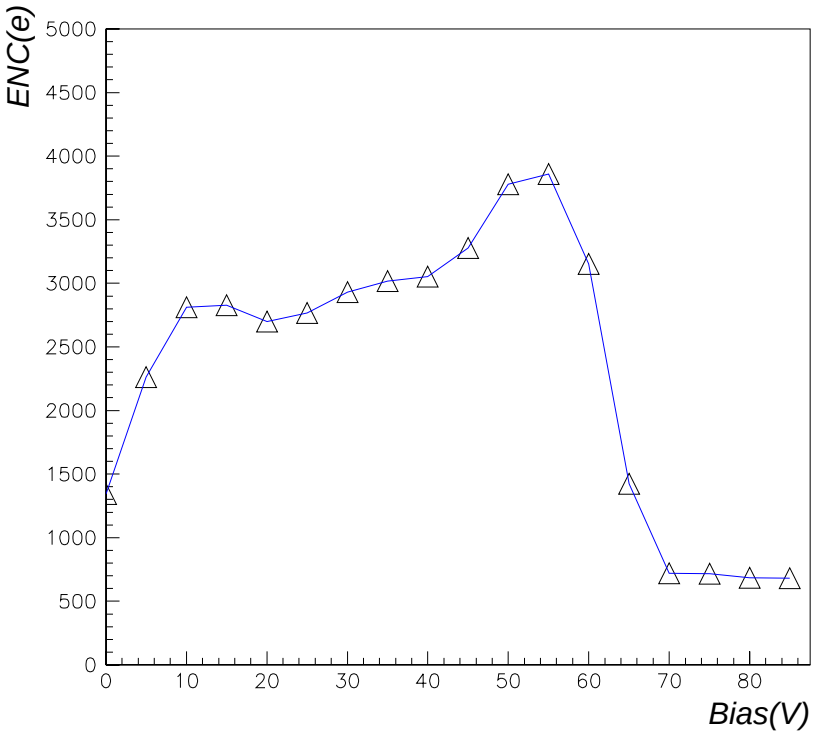


Figure 5.7: VA1 noise with the DSSD vs. detector bias voltage.

point. If the TA were completely noise-free, the shape of the result should look like a step function. In reality, the shape is smeared by the noise as shown in Fig. 5.10. Assuming the Gaussian for the noise distribution, we can fit the distribution by the integrated Gaussian,

$$f(x) = N \int_0^x G(t;\mu,\sigma)dt \tag{5.1}$$

$$G(t;\mu,\sigma) = \frac{1}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(t-\mu)^2}{2\sigma^2}\right), \tag{5.2}$$

where x is the injected charge, N is the number of the injected pulses, μ and σ are the threshold and the noise, respectively.

We measure the real threshold by changing the threshold parameter *Vthr*. Figure 5.11 (a) shows the measured threshold for the shaping time = 300 ns and positive test pulse. The horizontal and vertical axes are the nominal threshold and the measured threshold. The nominal threshold is determined by the threshold parameter

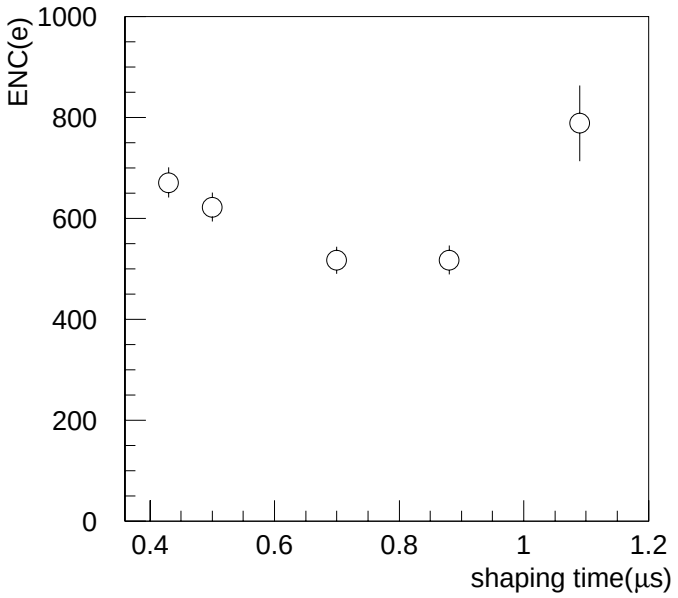


Figure 5.8: VA1 part noise with the DSSD vs. shaping time.

Vthr as shown in Table 5.1. For the nominal threshold below 3000 e^-, the results are affected by a noise triggering. We can see the threshold changes linearly for the nominal threshold above 3000 e^-. The measured noise is 800 e^- as shown in Fig. 5.11 (b).

Figure 5.11 (c) shows the shaping time = 75 ns and positive test pulse result. We can also see the threshold changes linearly. In the case of the shaping time = 75 ns, a gain degradation of the shaper is observed, i.e. for a given threshold more input charge is needed to trigger the channels than the case of the shaping time = 300 ns. The measured noise is 1180 e^- as shown in Fig. 5.11 (d).

For the negative test pulse, we cannot measure the threshold with the normal set of the bias parameters. The large noise in the negative test pulse is considered to cause this problem. The tuning of the bias parameter *vrc* of the high-pass filter is necessary to avoid the noise effect. We set *vrc* = +3, which makes the cutoff frequency of the high-pass filter the highest. Figures 5.12 (a) and (c) show the results of negative test pulse with the shaping time = 300 ns and 75 ns, respectively. We can see the threshold changes linearly for the nominal threshold above 6000 e^-. As shown in Figs. 5.12 (b) and (d), the noise changes linearly at the negative test input. We need a further investigation to understand the origin.

The TA part is further evaluated by connecting it to the ohmic side strips of

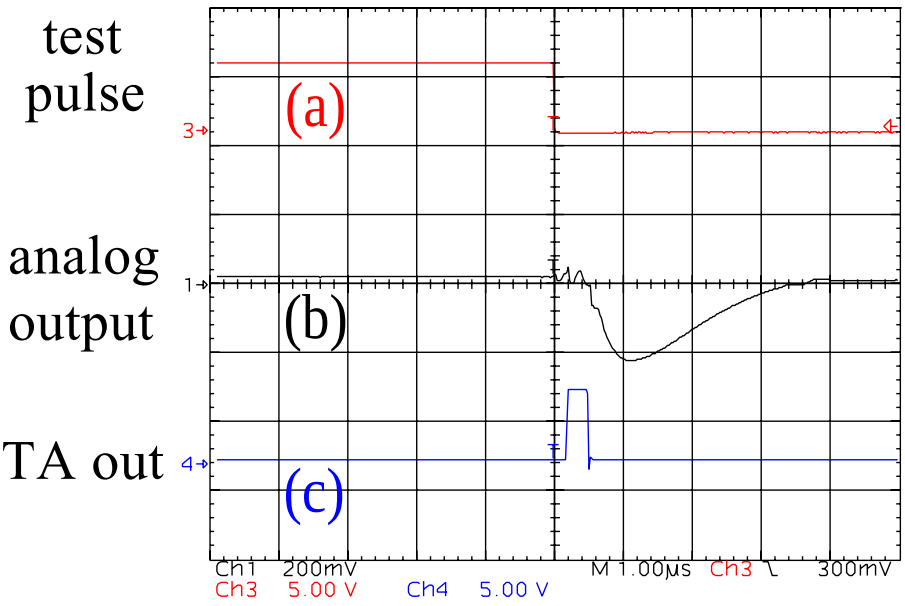


Figure 5.9: Outputs from VA1TA. (a), (b), and (c) lines are the test pulse, the analog output, and the TA output, respectively.

the DSSD. Figure 5.13 shows the measured threshold and noise as a function of the nominal threshold. For the nominal threshold below 5000 e^-, the results are affected by a noise triggering. We can see the threshold changes linearly over the nominal threshold = 5000 e^-.

We check the threshold and noise distributions of the TA by changing the bias parameters listed in Table 5.2 ("obi", "Pre_bias", "sbi", "vrc", "Ifp", and "Ifsf"). The results are shown in Fig. 5.14 and Fig. 5.15. From these results, we conclude that the "Pre_bias", "sbi", "vrc", and "Ifsf" parameters change the threshold level of the discriminator largely. We can tune the threshold of the TA using these parameters.

5.4.2 Trigger Timing

The TA asserts the trigger signal before the input signal reaches the peak. Since the pulse height of the fast shaper output is unstable due to the noise of the TA part, input charge difference, and channel-by-channel gain difference, the trigger timing depends on the pulse height of the fast shaper output (as shown in Fig. 5.16). We evaluate the dependence of the TA output timing on the signal pulse height.

For this measurement, we probe the test pulse and the trigger output on the VA-

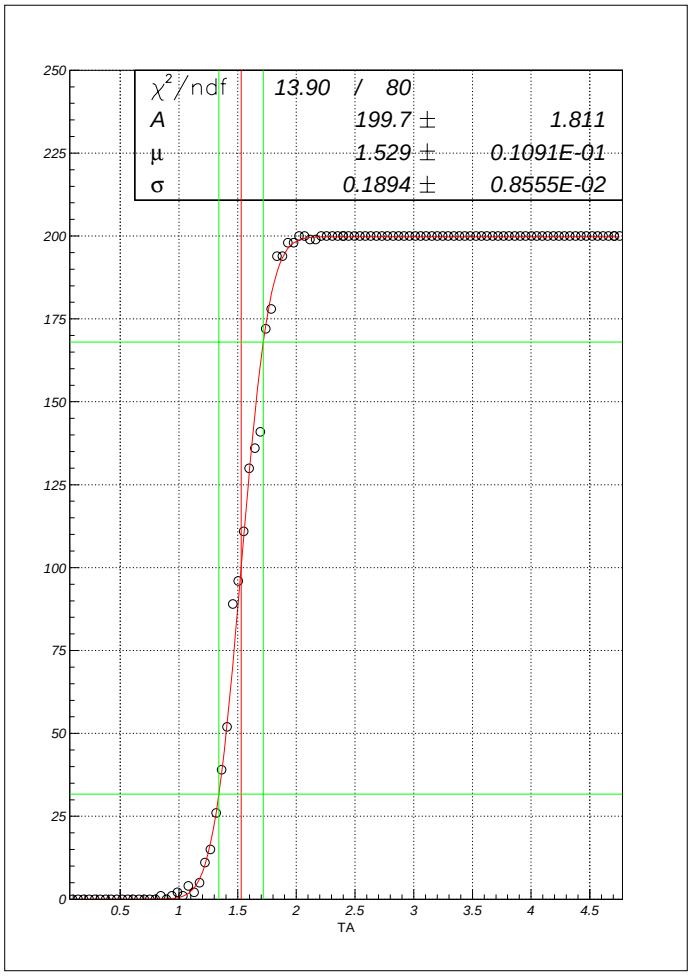


Figure 5.10: An example of the threshold fit. The horizontal and vertical axes are the injected charge and number of the triggered events, respectively.

DAQ. Since there are some ADCs, buffers, etc., the measured delay time contains the delay due to these chips. When a large enough signal comes in the VA1TA chip, the trigger signal from the TA part must be asserted immediately. The measured delay time on the VA-DAQ is 165 ns for the shaping time = 300 ns, nominal threshold = 2000 e^- and input charge above 65000 e^-. We assume this value as the delay due to the buffers, and subtract it from the measured values.

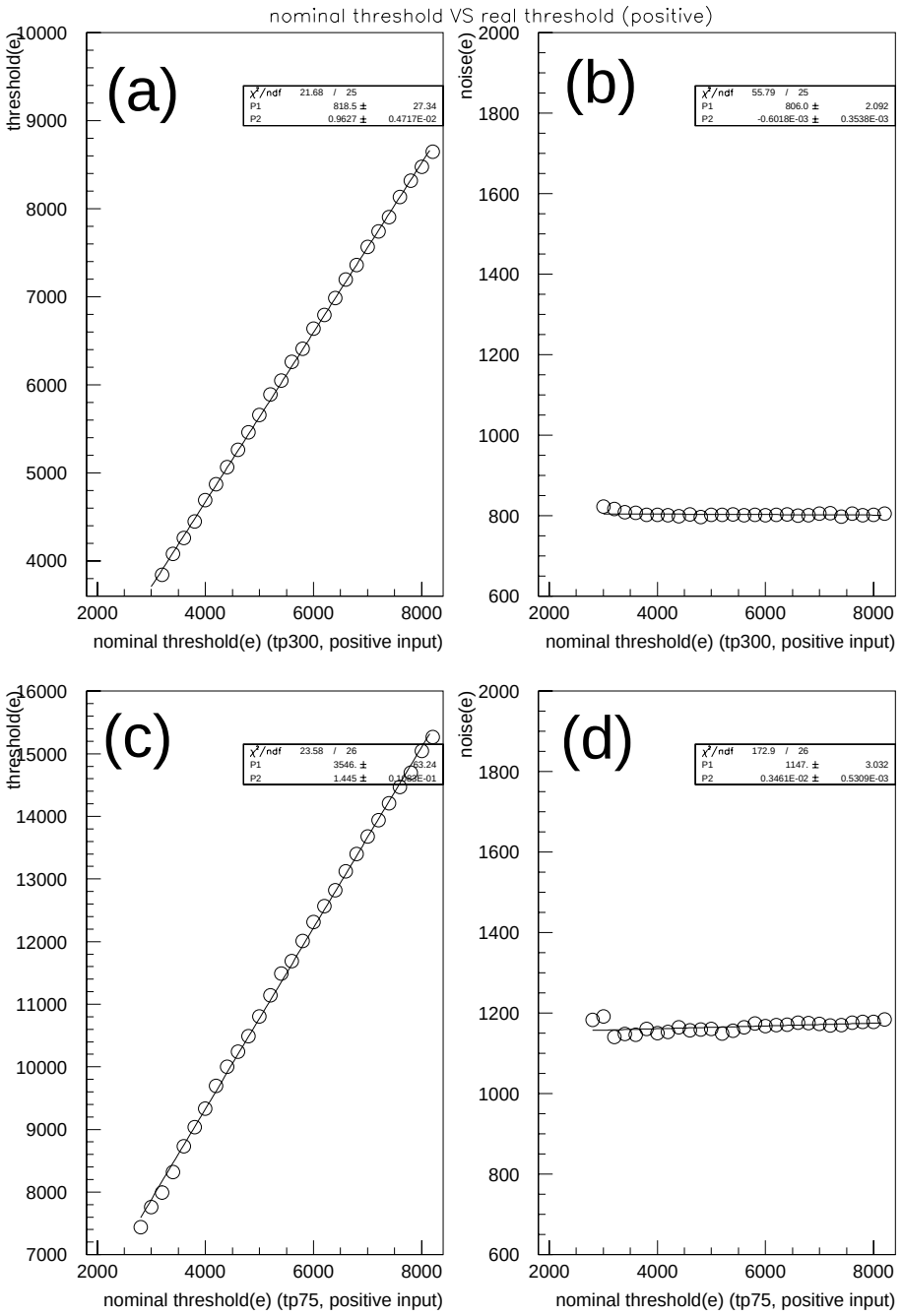


Figure 5.11: Measured threshold and noise as a function of the nominal threshold (positive input). (a) and (b) are the threshold and the noise for the shaping time = 300 ns, respectively. (c) and (d) are the threshold and the noise for the shaping time = 75 ns, respectively.

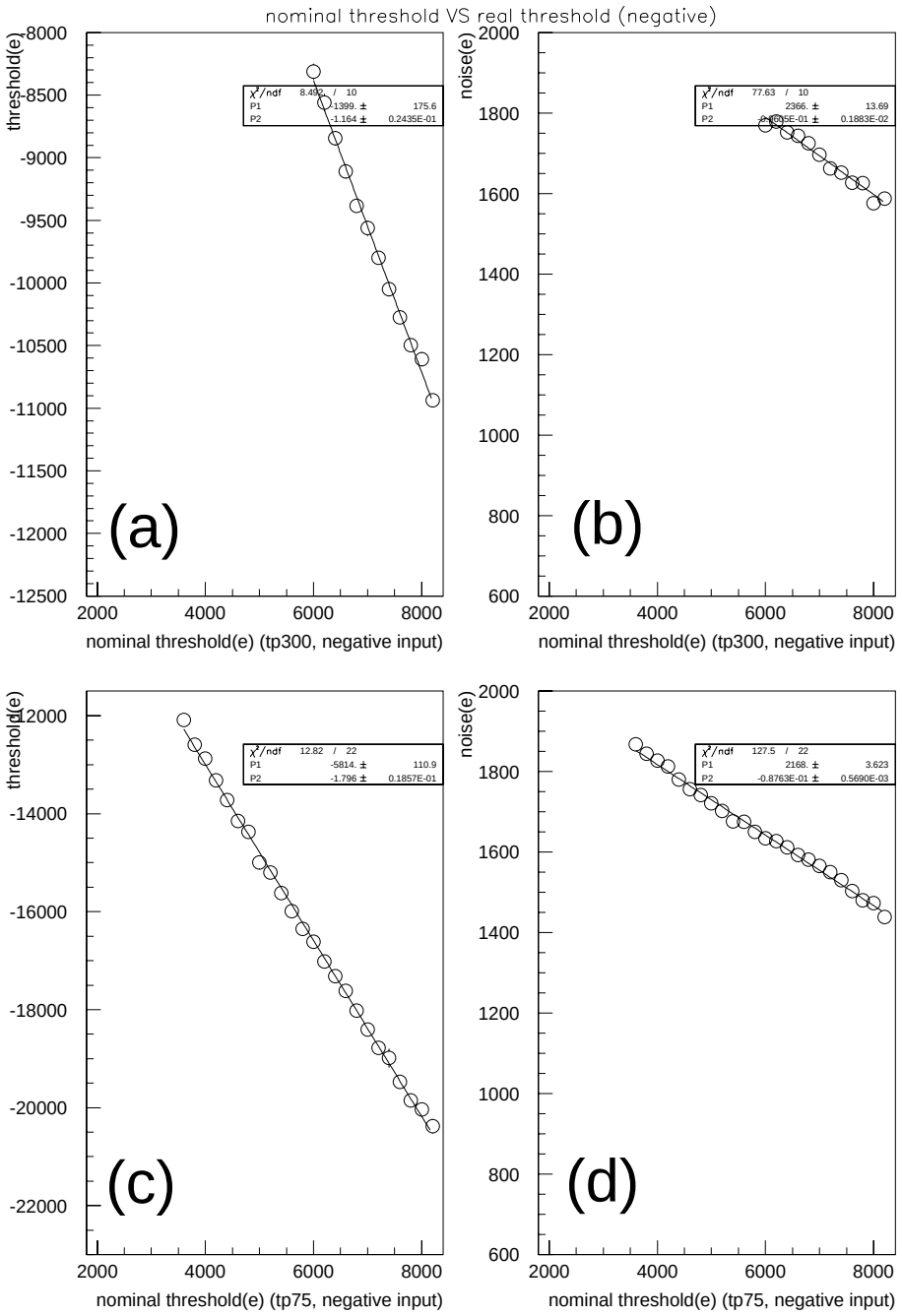


Figure 5.12: Measured threshold and noise as a function of the nominal threshold (negative input). (a) and (b) are the threshold and the noise for the shaping time = 300 ns, respectively. (c) and (d) are the threshold and the noise for the shaping time = 75 ns, respectively.

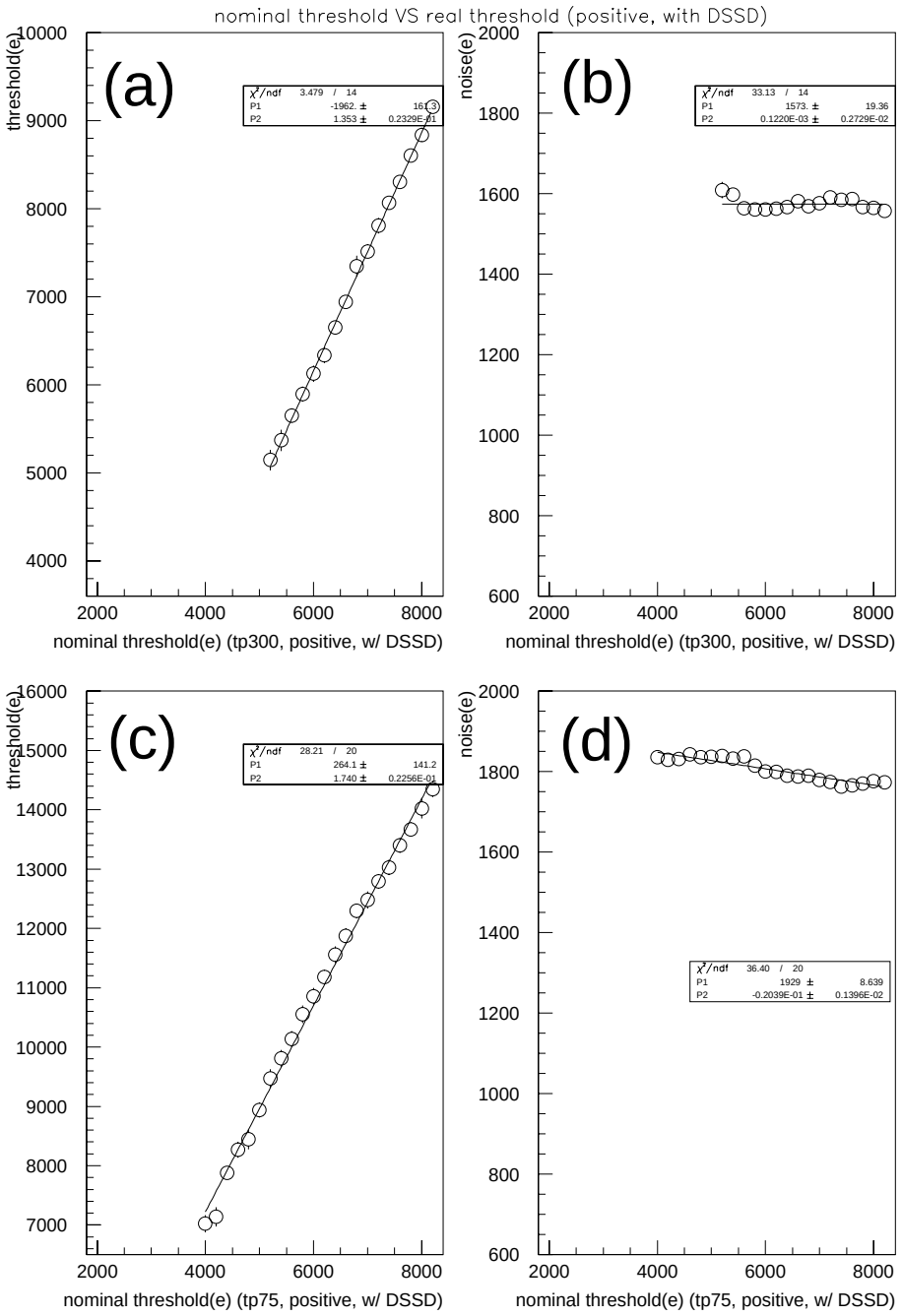


Figure 5.13: Measured threshold and noise as a function of the nominal threshold (positive input, with DSSD). (a) and (b) are the threshold and the noise for the shaping time = 300 ns, respectively. (c) and (d) are the threshold and the noise for the shaping time = 75 ns, respectively.

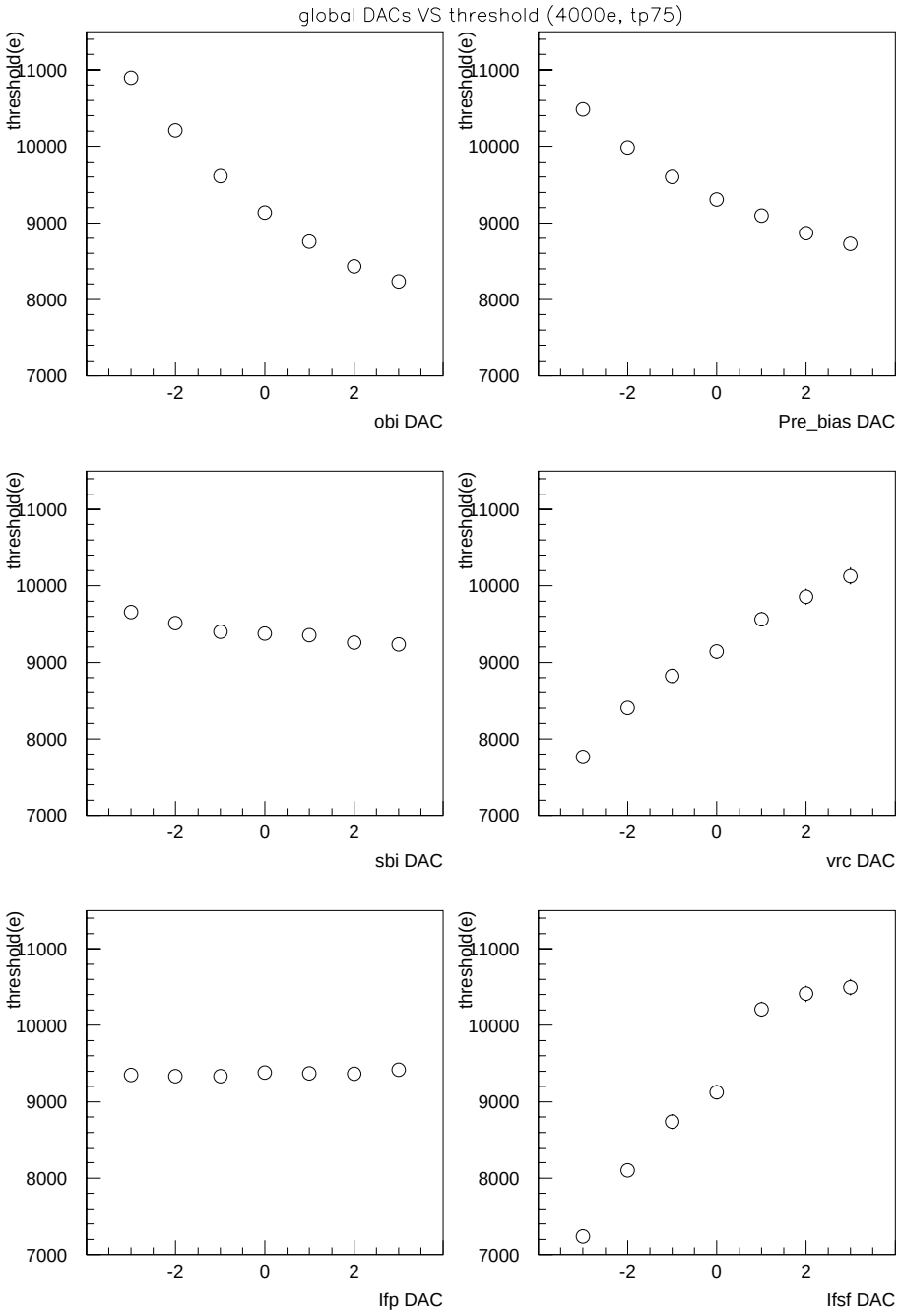


Figure 5.14: Measured threshold vs. bias parameters (nominal threshold=4000e, shaping time=75 ns)

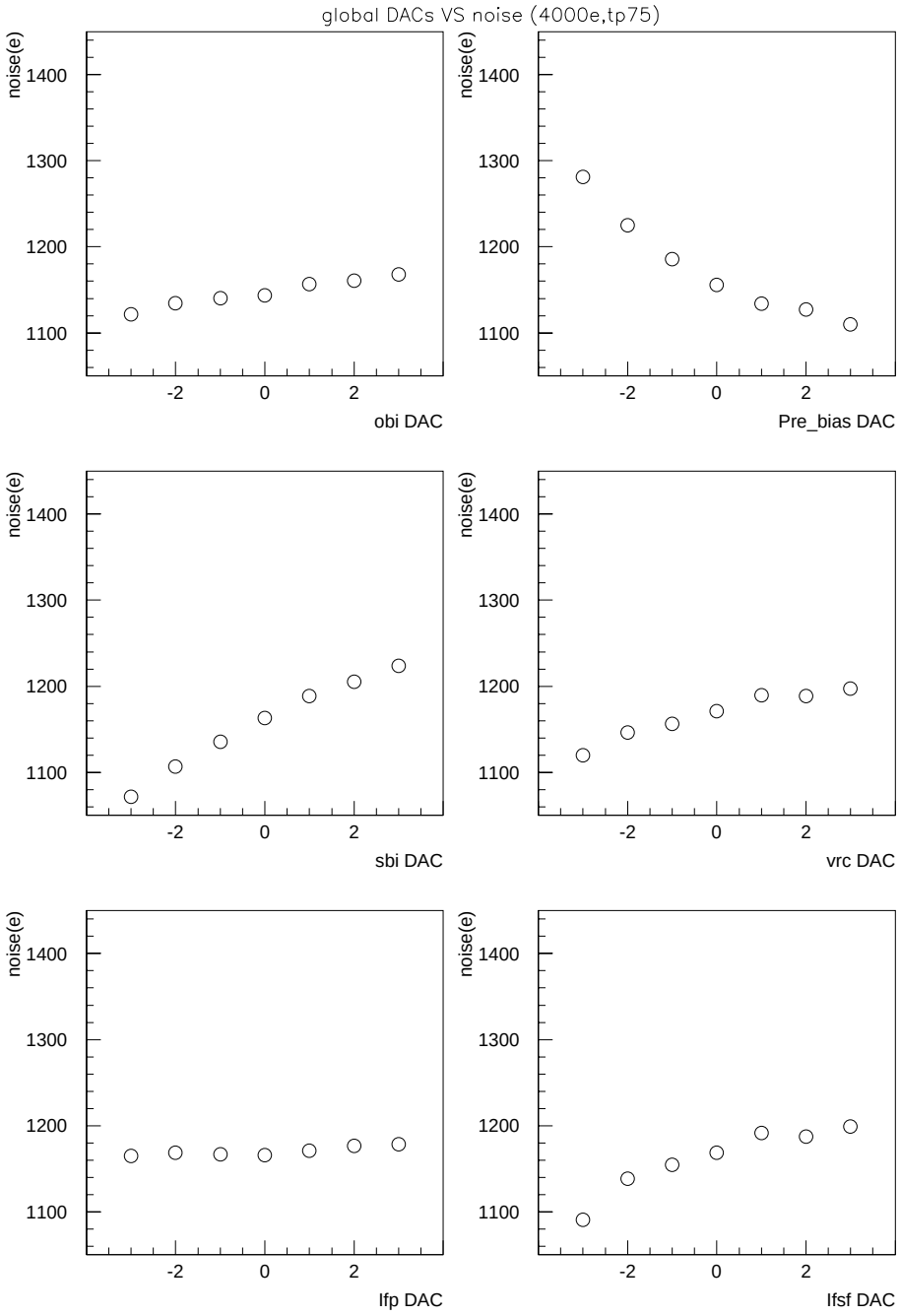


Figure 5.15: Measured noise vs. bias parameters (nominal threshold=4000e, shaping time=75 ns)

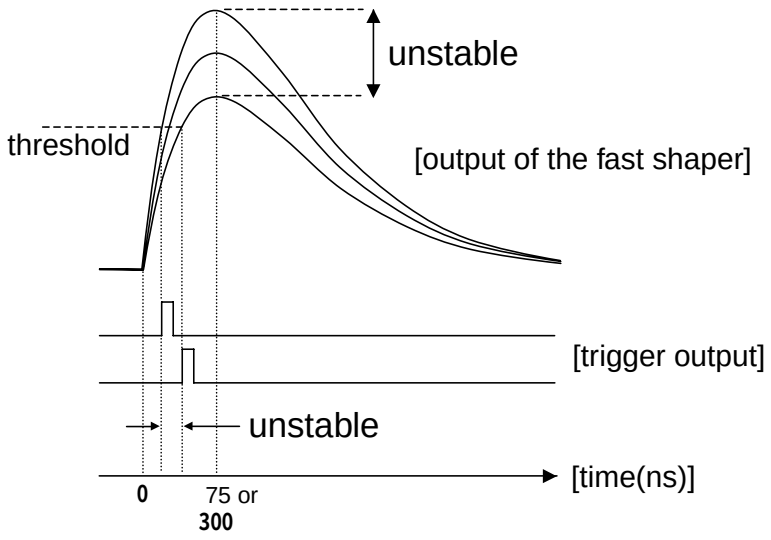


Figure 5.16: Trigger signal output timing. The timing is somewhat unstable due to the noise, the input charge difference and the gain difference (channel-by-channel).

5.4.2.1 Delay Time Dispersion

We evaluate the delay time dispersion in one chip. Figure 5.17 shows the measured delay time for the shaping time = 300 ns, the input charge = 12300 e^-. The measured dispersion are 6 ns and 12 ns for the nominal threshold = 4000 e^- and 8000 e^-, respectively.

Figure 5.18 shows the measured delay time for the shaping time = 75 ns, the input charge = 18500 e^-. The measured dispersion are 3 ns and 6 ns for the nominal threshold = 4000 e^- and 8000 e^-, respectively.

5.4.2.2 Threshold Dependence

We evaluate the delay time (latency) performance and functionality of the nominal threshold DAC value for one channel.

Figure 5.19 (left) shows the measured latency of the TA as a function of the nominal threshold for the shaping time = 300 ns, test pulse = 12300 e^-. Figure 5.19 (right) shows the measured latency of the TA as a function of the nominal threshold for the shaping time = 75 ns, the test pulse = 18500 e^-. (These input charges are selected so that the TA triggers for all the nominal threshold settings. See Fig. 5.11.)

The standard deviations of the delay time at the nominal threshold = 4000 e^-

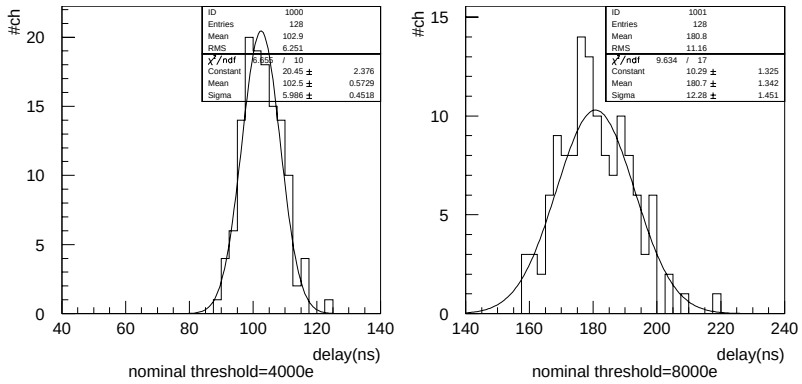


Figure 5.17: Measured delay for the shaping time=300 ns. The left and right figures show the nominal threshold = 4000 e^- and 8000 e^- cases, respectively.

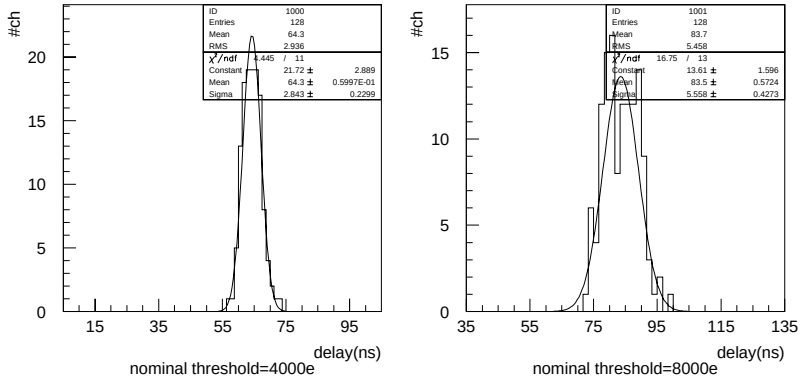


Figure 5.18: Measured delay for the shaping time=75 ns. The left and right figures show the nominal threshold = 4000 e^- and 8000 e^- cases, respectively.

are 16 ns and 7 ns for the shaping time = 300 ns and 75 ns, respectively. The deviations increase when larger threshold is selected. (For example, at the nominal threshold=8000 e^-, the deviations are 27 ns and 14 ns for the shaping time = 300 ns and 75 ns, respectively.)

5.4.2.3 Bias Parameters Dependences

As described in Sec. 5.4.1, the threshold level of the discriminator depends on some of the bias parameters. Therefore the delay time should also depend on the bias parameters. Figure 5.20 shows the measured latency for the TA as a function of the bias parameters for the shaping time = 75 ns, the test pulse = 18500 e^-, and the

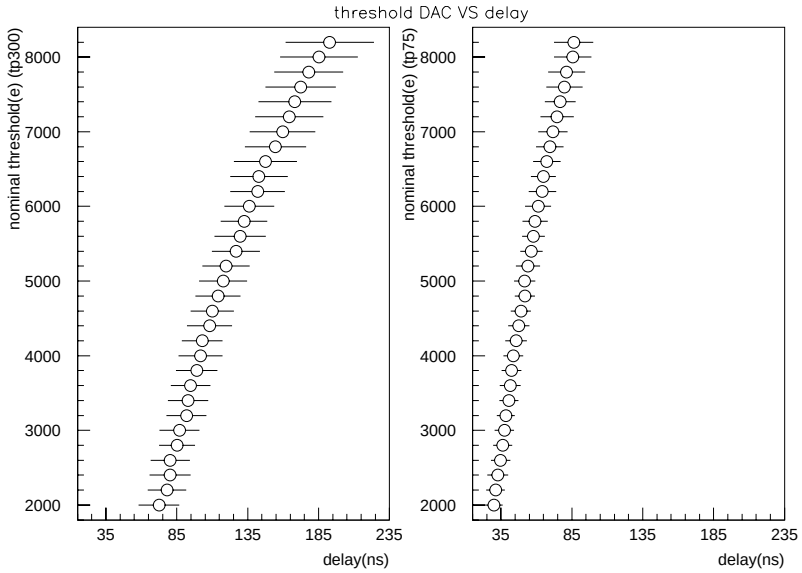


Figure 5.19: Measured delay vs. nominal threshold DAC value. The left and right figures show the shaping time = 300 ns and 75 ns cases, respectively.

nominal threshold=4000 e^-.

5.4.2.4 Input Charge Dependence

We check the input charge dependence of the delay time for one channel. Figure 5.21 shows the relation between the measured delay time and the input charge. The left and right figures show the shaping time = 300 ns and 75 ns cases, respectively.

At the nominal threshold = 4000 e^- case, the measured thresholds are 5500 e^- and 10500 e^- for the shaping time = 300 ns and 75 ns, respectively.

5.4.2.5 Summary of the Timing Tests

Table 5.6 summarizes the measured results with the nominal threshold = 4000 e^-, the input charge = 12300 e^- and 18500 e^- for the shaping time = 300 ns and 75 ns, respectively. The trigger signal from the TA part is asserted within the shaping time (75 ns or 300 ns), and the measured dispersions are small enough, $\sim$ 10 ns for the shaping time = 75 ns. If we use the shaping time for 75 ns, the VA1TA satisfies the required latency, $<$ 125 ns, for the SVD self-trigger.

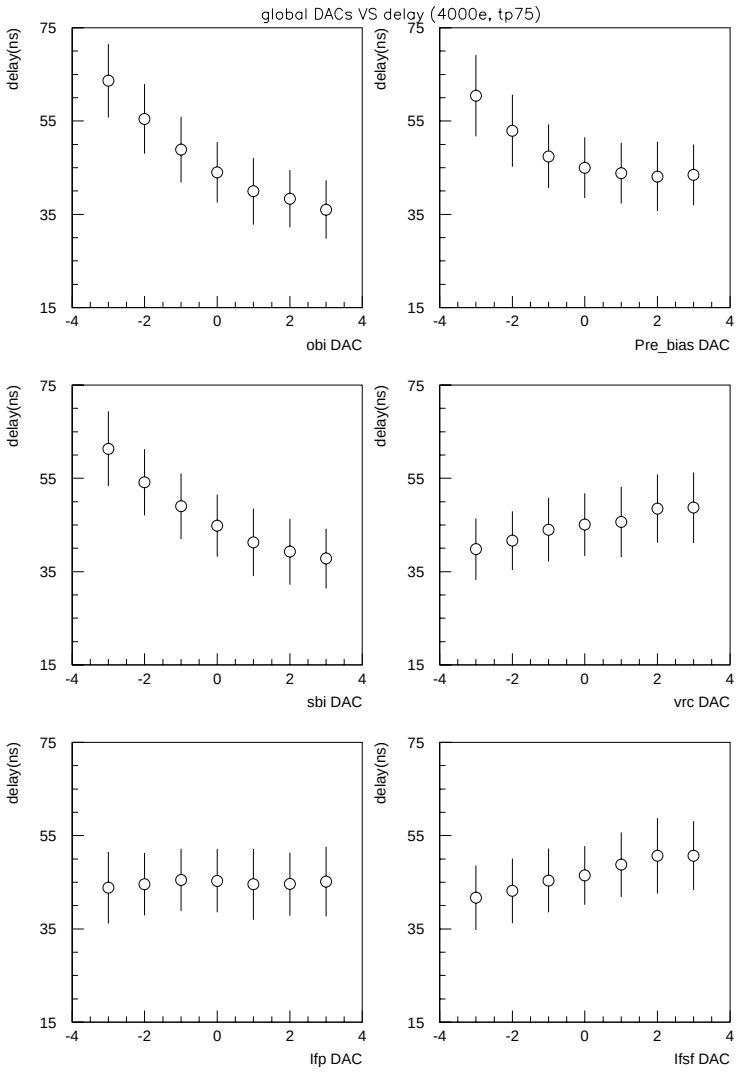


Figure 5.20: Measured delay vs. bias parameters (nominal threshold=4000e, shaping time=75 ns)

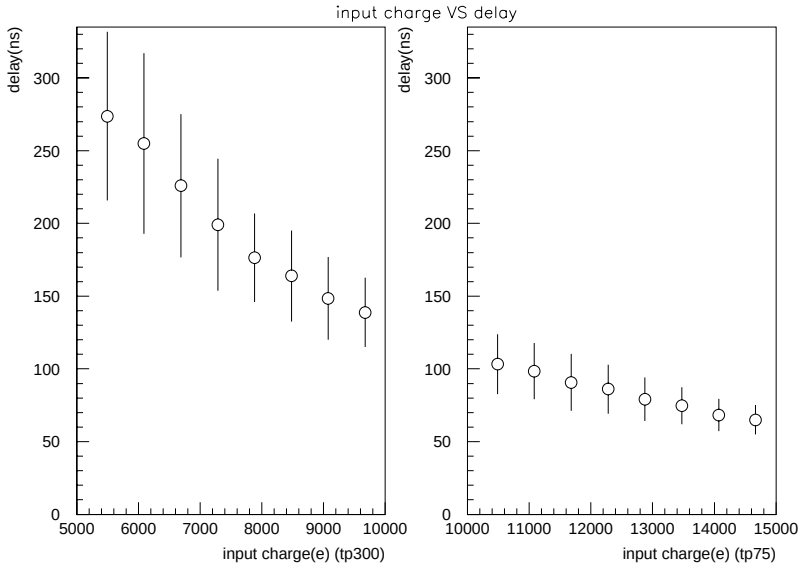


Figure 5.21: Measured delay time vs. input charge. (nominal threshold=4000 e^-) The left and right shows the shaping time = 300 ns and 75 ns cases, respectively.

5.4.3 Trigger Threshold Optimization

5.4.3.1 TA Tuning

As described in Sec. 5.4, in the case of the shaping time (fast) = 75 ns, for a given threshold more input charge is needed to trigger the channels than the nominal threshold. However, we can lower the threshold level of the discriminator using the bias parameters. Since the parameters "Ifsf", "vrc", "prebias", and "obi" affect the threshold level, we set these parameters in order to lower the threshold level as ifsf=−3, vrc=−3,

Table 5.6: Summary of the measured latency (ns) with the nominal threshold = 4000 e^-, the input charge = 12300 e^- and 18500 e^- for the shaping time = 300 ns and 75 ns, respectively.

measurement	shaping time = 300 ns	shaping time = 75 ns
dispersion (chip)	6 ns	3 ns
dispersion (channel)	16 ns	7 ns
dispersion (total)	17 ns	8 ns

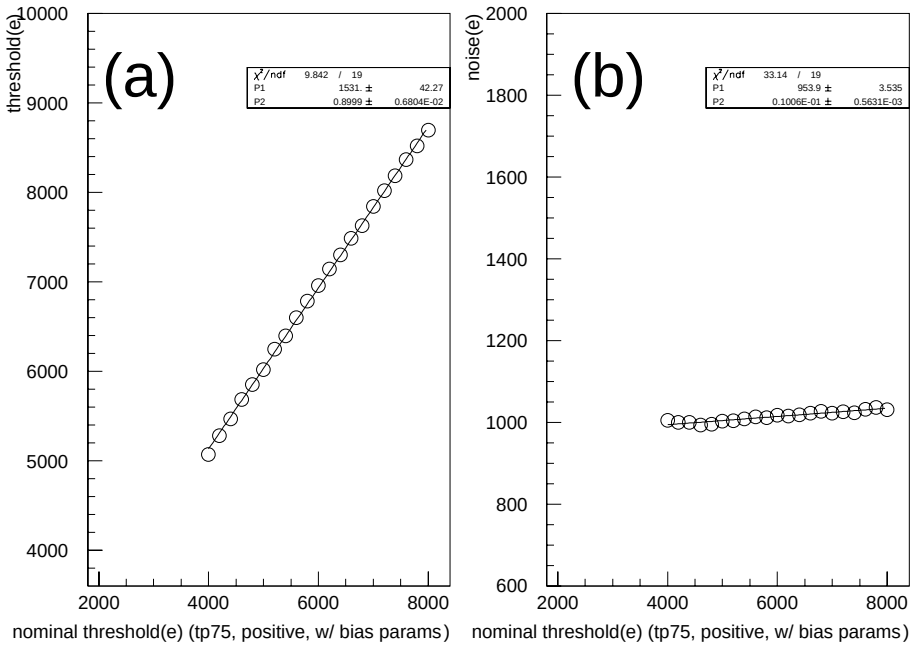


Figure 5.22: Measured threshold vs. nominal threshold. (shaping time=75 ns, positive input, with the set of the optimized bias parameters.)

prebias=+3, and obi=+3, and we check the threshold (the shaping time=75 ns, positive input). Figure 5.22 shows the relation between the measured threshold and the nominal threshold. Comparing with Fig. 5.11 (c), we can see a clear threshold decrease. The lowest threshold is measured to be 5000 e^-, which corresponds to the 1/4 of the most-probable peak height, 19000 e^-.

However, as shown in Fig. 5.20, the delay time is changed by some bias parameters. We check the delay time changing the input charge with the similar parameter setting, ifsf=−3, vrc=−3, prebias=+3, obi=+3, and sbi=+3. The "sbi" parameter does not affect the threshold level, but changes the delay time. Figure 5.23 shows the relation between the measured delay time and the input charge in one channel. The measured threshold in this situation is about 5200 e^- with the nominal threshold = 4000 e^-.Comparing the result with Fig. 5.21, we see the shaping time of the fast shaper changes about 20 ns. This also satisfies the required delay time, < 125 ns. From this result, we find that the use of the bias parameters enables us to tune the threshold level keeping the shaping time of the fast shaper.

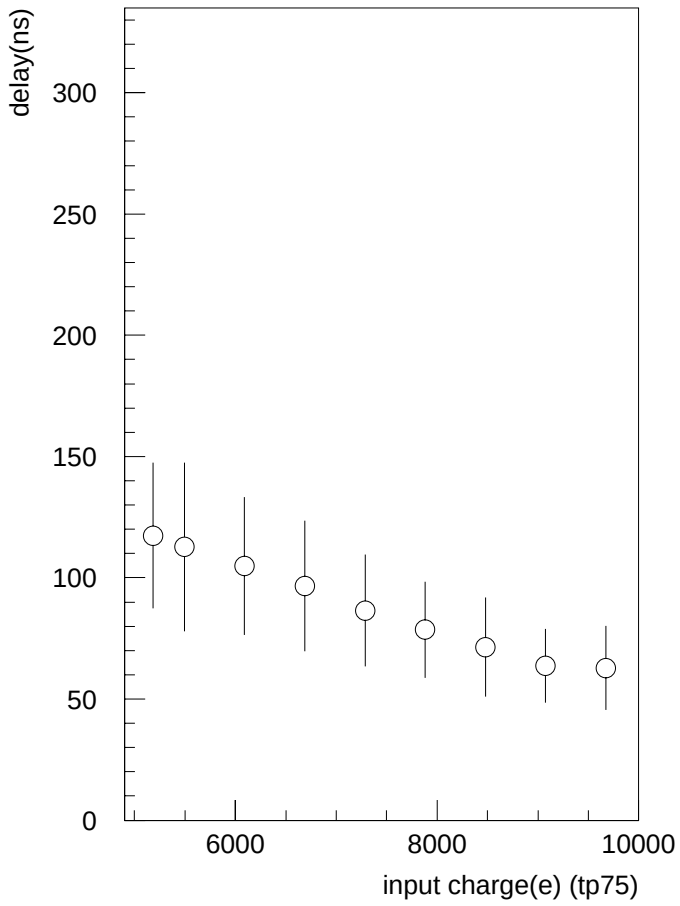


Figure 5.23: Measured delay vs. input charge. (nominal threshold=4000e, shaping time=75 ns)

5.4.3.2 Threshold Optimization

To set the threshold of TA, we can also use the "internal trim DAC". The trim DAC changes the threshold voltage of each discriminator channel-by-channel.

First, we measure the threshold linearity by changing the trim DAC value. Figure 5.24 shows the measured threshold difference between the thresholds before and after changing the trim DAC value as a function of the trim DAC value for one channel. Threshold difference decreases in proportion to the trim DAC value. The decrease constant is measured to be -156 [e^-/bit].

We evaluate the threshold dispersion before and after setting the trim DACs. Figure 5.25 shows the measured dispersion for one chip. Since the trim DAC value changes the threshold linearly, we set the trim DAC value for each channel as shown

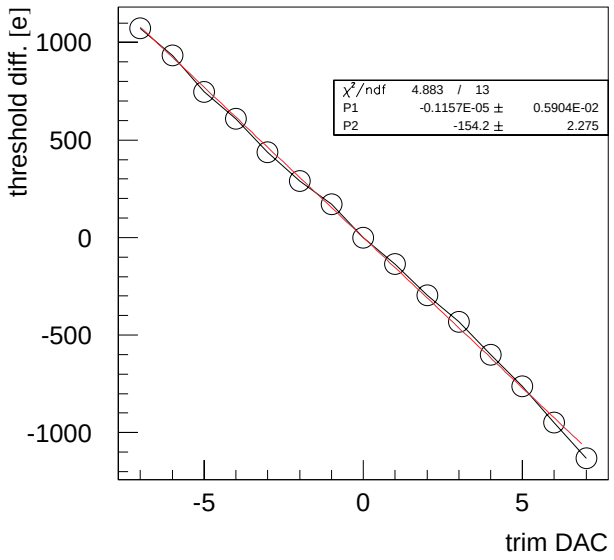


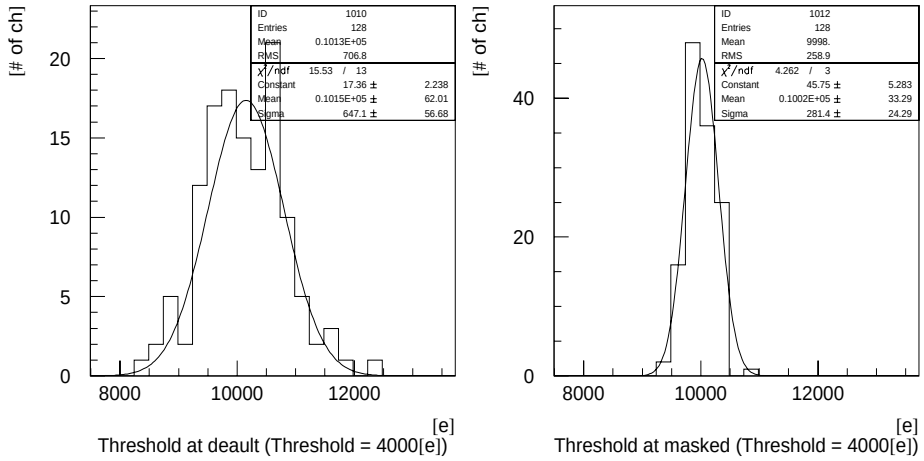
Figure 5.24: Threshold difference from default value as a function of the trim DAC value.

in Table 5.7. In addition, the sum of all the trim DAC values must be nearly zero for one chip to keep the total threshold value constant. After using trim DACs, the standard deviation of the threshold in one chip is about 300 e^-. This satisfies the specification value, 200 $\sim$ 400 e^-. This value is much smaller than the measured noise of the TA, 1000 e^-.

We check the delay time dispersion using the trim DACs. Figure 5.26 shows the measured delay time for the shaping time = 75 ns, the input charge = 18500 e^-. The measured dispersion of the delay time is 3.5 ns. This value is smaller than the previous value, 6 ns.

Table 5.7: Trim DAC setting.

Applied trim DAC value	Difference from average value (e)
-7	~ -1014
-6	$-1014 \sim -858$
-5	$-858 \sim -702$
-4	$-702 \sim -546$
-3	$-546 \sim -390$
-2	$-390 \sim -234$
-1	$-234 \sim -78$
0	$-78 \sim 78$
1	$78 \sim 234$
2	$234 \sim 390$
3	$390 \sim 546$
4	$546 \sim 702$
5	$702 \sim 858$
6	$858 \sim 1014$
7	$1014 \sim$



(a) Before (b) After

Figure 5.25: Threshold dispersion before and after using the trim DACs in one chip.

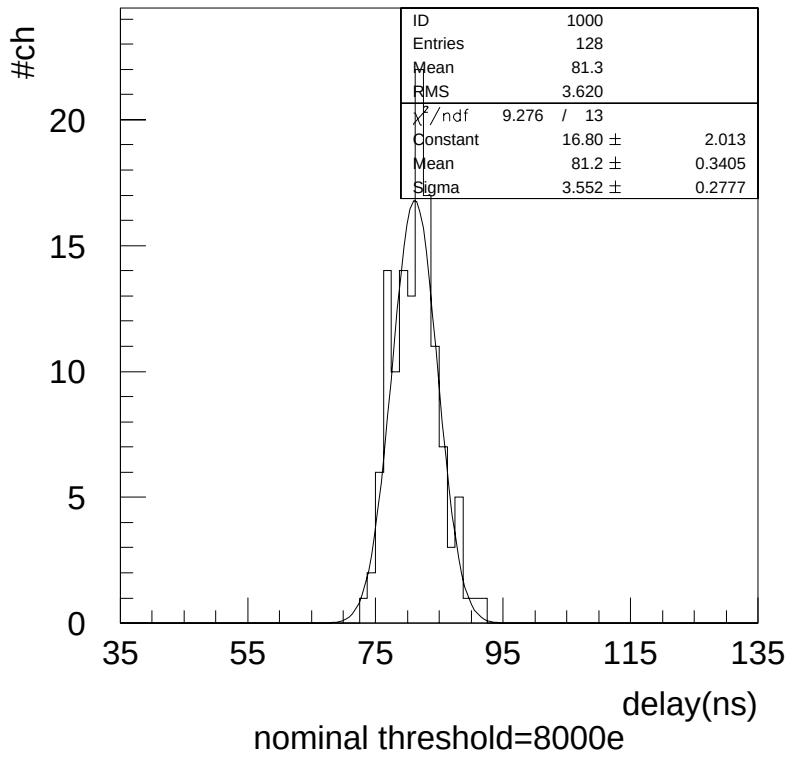


Figure 5.26: Measured delay for the shaping time setting=75 ns, nominal threshold=8000 e^-.

Chapter 6

Conclusion

We have developed a new silicon strip readout chip, the VA1TA, for the upgraded Silicon Vertex Detector (SVD) of the Belle experiment. The VA1TA provides a fast trigger signal which can be used to trigger the SVD.

The noise of the analog output connected with the DSSD is measured to be 520 e^- at peaking time = 0.7 μs. This corresponds to the S/N ratio of 36 and satisfies the requirement. We confirm that the threshold of the trigger discriminator can be set as low as 5000 e^- with the peaking time of 75 ns by optimizing the bias parameters. The standard deviations of the delay time are measured to be 3.5 ns in a chip and 7 ns in a channel with the peaking time = 75 ns, the threshold = 5000 e^-, and the input charge = 18500 e^-. We confirm that the VA1TA provides a fast trigger signal for less than 75 ns after the event occurred. The dispersion of the threshold level in a chip can be minimized to be 300 e^- by optimizing the threshold level channel-by-channel.

We have some problems in the measurement of the trigger performance with the negative test pulse. Although these problems are considered to be due to a large noise in the test pulse, we need a further investigation to understand the origin.

From these results, we conclude that the performance of the VA1TA chip is satisfactory for the upgraded SVD of the Belle experiment.

Appendix A

Principle of Silicon Strip Detector

The semiconductor detectors, originally used for the energy measurement of an ionizing particle in nuclear physics, are now widely used in particle physics experiments. In particular, their capabilities of a precise position measurement make the silicon detectors very popular device in particle physics experiment in which accurate position measurement is required.

In this chapter, the fundamentals of the semiconductor devices and the principle of the silicon strip detector are described.

A.1 Semiconductor Device Basics

In a perfect crystal, electron energies are constrained to lie in bands. The valence band and conduction band are separated by an energy gap in which no electrons are allowed. The electrons in valence band are excited thermally to conduction band. The electrons missing in the valence band are called holes. For an intrinsic semiconductor, the number of electrons is equal to the number of holes.

The semiconductors are usually doped with small fraction of impurities to produce additional states in the originally forbidden energy gap. The impurity atoms with one additional electron in the outer shell (e.g. phosphorus or arsenic) are called "donor" and those with one less valence electron (e.g. boron in silicon) called "acceptor". In the n-type (doped with donor atoms) semiconductors, almost all electrons from donor states situated close to conduction band move into the conduction band because of the high density of available free states in the band. This causes a shift of the Fermi level from the gap center toward the conduction band and a decrease in the density of

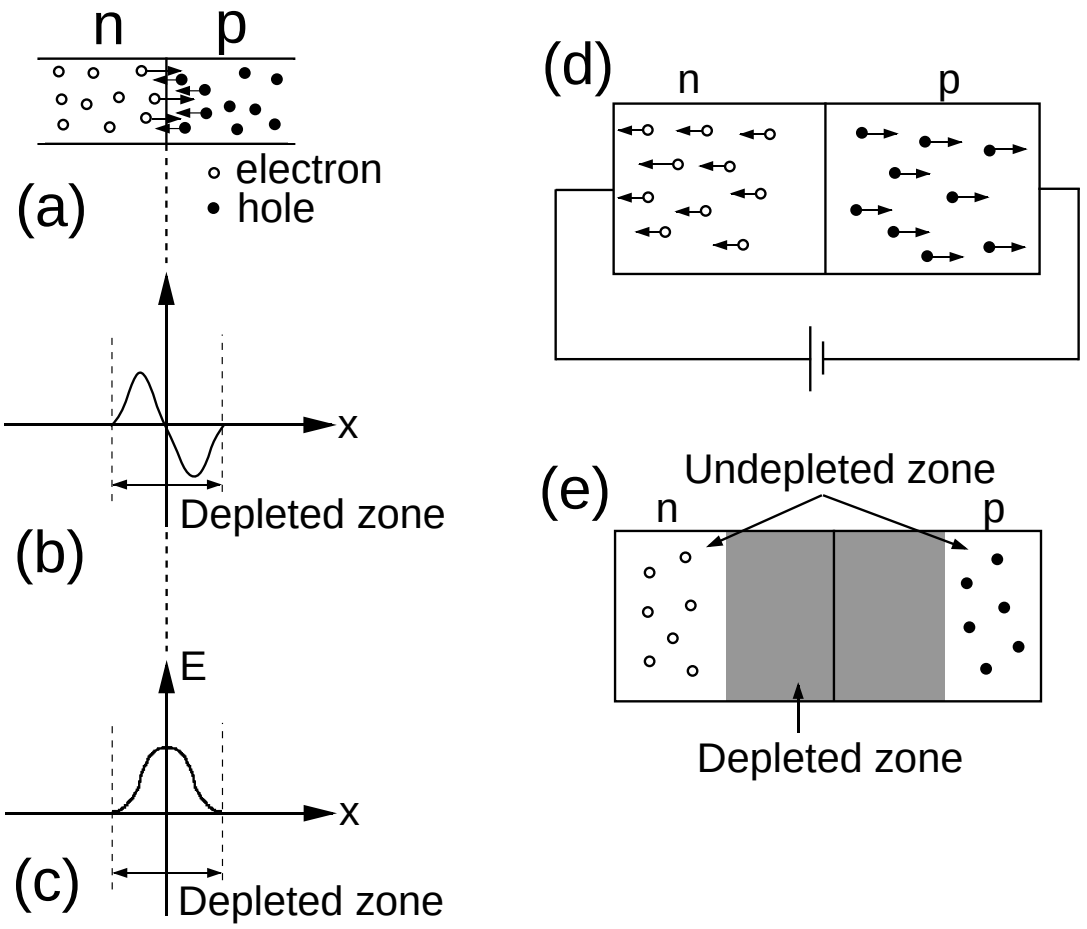


Figure A.1: Schematic drawing of the p-n junction.

the holes in the valence band. In the p-type (doped with acceptor atoms) materials, an increase of the hole densities and a decrease of the electron densities are caused by similar effects.

p-n Junction The band structures of the p and n semiconductors are shown in Fig. A.1(a). Once they are brought into contact, the electrons and holes drift into the p-region and the n-region, respectively. This causes an excess of the negative charge in the p-region and the positive charge in the n-region. As a result, the electric field is created and any movable charge carriers (electrons and holes) are swept out from the region around the boundary, resulting in a space charge region. Figures A.1(b) and (c) show the carrier density and the electric field distributions, respectively.

If the negative voltage on the n-side and the positive voltage on the p-side are applied, the movable charge carriers are pushed toward the junction, and the electrons and holes recombine near the interface and current flow. When the voltage in the opposite direction is applied, the electrons and holes are pulled away and the space charge region increases as shown in Figs. A.1(d) and (e).

A.2 Silicon Strip Detector

Strip detectors are in principle large area diode divided into the narrow strips, each of which is read out by a separate electronic circuit. The detector consists of a highly doped p^+ region on a low doped n^- substrate, the backside of a highly doped n^+ layer. Usually, a reversed bias is applied to fully deplete the substrate, making the sensitive area wider and the number of produced charge greater.

The charged particles passing through the detector ionize atoms in the depletion region to produce electron-hole pairs. The generated electrons and holes are separated by the strong electric field and the electrons (holes) drift towards n^+ (p^+) electrode. The position of the charged particle is given by the location of the strip carrying the signal. The signal from the detector is read out as amount of the charge collected in the electrode. It is converted into the voltage by a charge amplifier and sent to the ADC.

The nominal thickness of a silicon strip detector is 300 μm and the required energy to produce an electron-hole pair is 3.6 eV in the silicon. A minimum ionizing particle deposits about 80 keV of its energy into a 300 μm thick silicon detector and creates about 22000 electron-hole pairs.

The single-sided strip detectors described above make use of only one type of the charge carrier, usually holes. By dividing the backside n^+ layer into the strips and using the electrons collected there, a second coordinate can be read out from the same wafer (Fig A.2). This is the principle of the double-sided silicon strip detector (DSSD). Since two-dimensional information can be obtained by one silicon wafer, we can reduce the effects of the multiple scattering by using the DSSD.

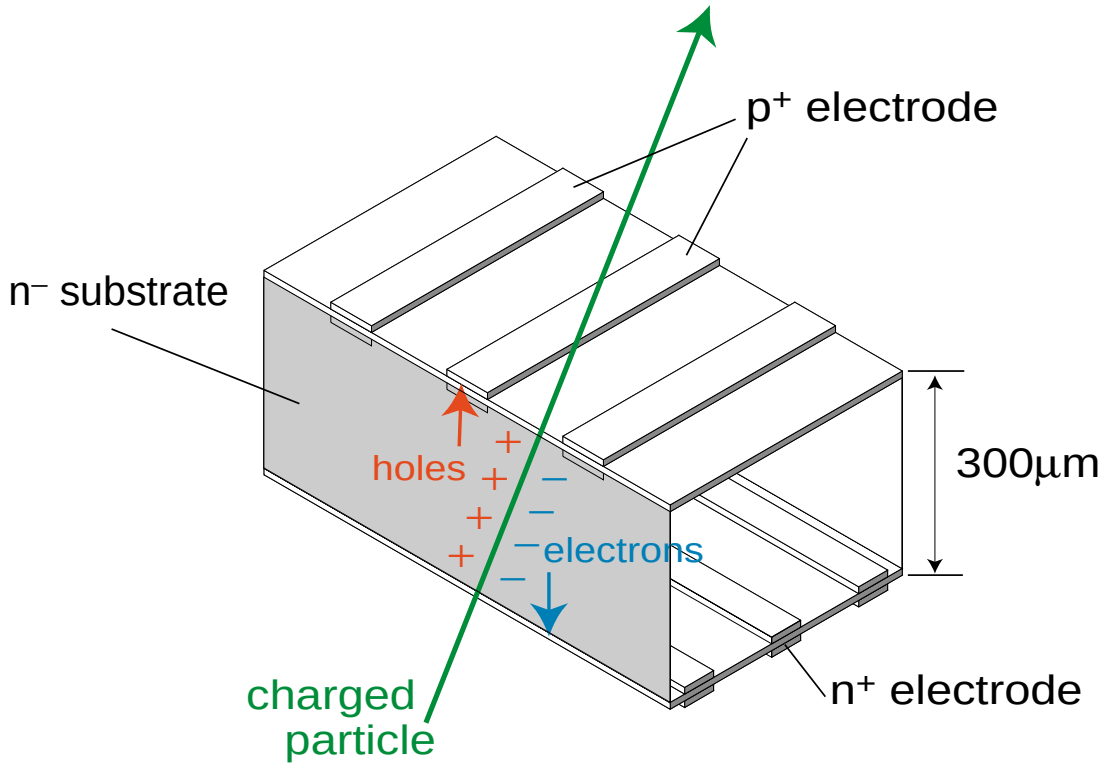


Figure A.2: Schematic drawing of the Double-sided Silicon Strip Detector (DSSD).

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