Construction and Performance of the Upgraded Silicon Vertex Detector for the Belle Experiment

Naohiko Uozaki
Department of Physics, University of Tokyo

January 10, 2003

Abstract

The Silicon Vertex Detector (SVD) for the Belle Experiment will be upgraded in summer 2003. Major improvement of the upgraded SVD is increase of layers from 3 to 4, smaller radius of the inner-most layer, larger angular acceptance, and better radiation tolerance.

We have developed a new procedure to assemble the modules (ladders) of SVD and successfully assembled all the necessary ladders.

We have tested SVD2 with the real readout system. S/N ratio is measured to be better than 10 for all layers, which satisfies our requirement. Using cosmic rays, we have shown that we are able to detect and reconstruct tracks. From these result, we have confirmed that the performance of SVD2 satisfies our requirements.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 CP Violation

Various symmetries play very important roles in particle physics. Some of them are continuous and the others are discrete. CP symmetry is one of the latter and the origin of its violation is one of the most exciting mysteries in the present particle physics. As its name indicates, the CP transformation is a product of two discrete operations, C and P.

Charge conjugation, C, is a symmetry between particles and antiparticles. The C invariance means that experiments in a world of antimatter will give identical results to the ones in our (of course, matter) world. Parity, P, is a symmetry of space. P invariance means that the mirror image of an experiment yields the same result as the original one.

Until 1956, it was believed that all elementary processes are invariant under C and P. Lee and Yang pointed out the possibility of the violation of these symmetries [1], and subsequent experiments [2] proved that C and P symmetries are really not conserved in weak interactions. However, the products of C and P transformations, CP was still considered to be a good symmetry.

The second impact came in 1964. An experiment using neutral K mesons showed that CP is also not conserved under weak interactions [3]. Neutral K mesons (K^0 and $\overline{K}^0$) are created by strong interactions. The mass eigenstates of the K^0 - $\overline{K}^0$ system can be written

$$|K_S>= p|K^0> +q|\overline{K}^0>, |K_L>= |K^0> -q|\overline{K}^0> \tag{1.1}$$

(choosing the phase so that $CP|K^0>= |\overline{K}^0>$). If the CP invariance held, we would have $q = p$ so that K_S would be CP even and K_L would be CP odd. Because the kaon is the lightest strange meson, it decays through the weak interaction. Neutral kaons can decay into two or three pions. Since pion has CP eigenvalue of -1, K_S always decays into three pions, if CP is conserved in weak interactions. The experiment performed at Brookhaven[1] proved that a small faction of K_L decays into two pions, which means CP is violated in the

weak interaction. In the kaon system, the order of observed CP asymmetry is of order 10^{-3}.

1.2 Cabbibo-Kobayashi-Maskawa Matrix

In 1973, M. Kobayashi and T. Maskawa proposed a theory of quark mixing which can introduce CP asymmetry within the framework of the Standard Model [4]. They demonstrated that quark mixing matrix with a measurable complex phase introduces CP violation into interactions.

In the Standard Model, the quark-W boson interaction part of the Lagrangian is written as

$$L_{qW} = \frac{g}{\sqrt{2}}\{\overline{u}_L \gamma_\mu W^+_\mu \mathbf{V} d_L + h.c.\} \tag{1.2}$$

where g is the weak coupling constant, $u_L(d_L)$ represents the left-handed component of u-type (d-type) quarks, and $\mathbf{V}$ is a quark-mixing matrix.

If all the elements of quark mixing matrix $\mathbf{V}$ are real, the amplitudes for a certain interaction and that for the CP conjugate interaction are the same. In order to violate CP, $\mathbf{V}$ should have at least one complex phase as its parameter.

In general, N dimensional unitary matrix has N^2 parameters, with $N(N-1)/2$ real rotation angles and $N(N+1)/2$ phases. Since we can rephase quark fields except one relative phase, $(2N-1)$ phases are absorbed and $(N-1)^2$ physical parameters are left. Among them, $N(N-1)/2$ are real angles and $(N-1)(N-2)/2$ are phases. The presence of phases means some of the elements must be complex and this leads to CP violating transitions.

For the case of $N = 2$, two quark-lepton generations, there is 1 rotation angle (the Cabbibo angle) and no phase. This means CP must be conserved in the model with four quarks.

For three generations, $N = 3$, there are three rotation angles and one phase so that CP can be violated. The quark mixing matrix for six-quark model can be written in many parameterizations, but two parameterizations are especially well known.

$$\mathbf{V} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \tag{1.3}$$

$$= \begin{pmatrix} c_{12}c_{13} & s_{12}c_{13} & s_{13}e^{-i\delta_{13}} \\ -s_{12}c_{23} - c_{12}s_{23}s_{13}e^{i\delta_{13}} & c_{12}c_{23} - s_{12}s_{23}s_{13}e^{i\delta_{13}} & s_{13}c_{13} \\ s_{12}s_{23} - c_{12}c_{23}s_{13}e^{i\delta_{13}} & -c_{12}s_{23} - s_{12}c_{23}s_{13}e^{i\delta_{13}} & c_{23}c_{13} \end{pmatrix} \tag{1.4}$$

$$\simeq \begin{pmatrix} 1 - \frac{1}{2}\lambda^2 & \lambda & A\lambda^3(\rho - i\eta) \\ -\lambda & 1 - \frac{1}{2}\lambda^2 & A\lambda^2 \\ A\lambda^3(1 - \rho - i\eta) & -A\lambda^2 & 1 \end{pmatrix} \tag{1.5}$$

The first parameterization, (1.4) is by Particle Data Group [5], where $c_{ij} \equiv \cos\theta_{ij}$ and $s_{ij} \equiv \sin\theta_{ij}$ for $i = 1, 2, 3$.

The second parameterization (1.5), originally by Wolfenstein [6], is also widely used. Setting λ to the sine of the Cabbibo angle [7], $\sin\theta_C \simeq 0.22$, and writing down all the elements in terms of powers of λ, the remaining three parameters are intended to be of order unity. It clearly indicates the hierarchy in the size of elements, the diagonal elements are almost unity, the elements between adjacent generations are smaller by an order of magnitude and the elements with the first and the third generations are further smaller. Experimentally, the parameters A and λ can be determined from tree-level decays and rather well known [5]:

$$A = 0.84 \pm 0.04, \qquad \lambda = 0.2196 \pm 0.0023 \tag{1.6}$$

while ρ and η are not determined precisely, since its determination requires the measurement of V_{ub} and V_{td} which are of order λ^3.

The unitarity of CKM matrix leads to some constraints on its elements. For example, the first and second columns lead to the equation

$$V_{ud}V_{us}^* + V_{cd}V_{cs}^* + V_{td}V_{ts}^* = 0 \tag{1.7}$$

which is related to the K meson system. Since the elements of CKM matrix are complex, this implies they form triangles on a complex plane. Although the unitarity of CKM matrix leads to six triangles, most of them have one side which is much shorter than the other two sides, and consequently one tiny angle. In Wolfenstein parameterization, one can compare the magnitudes of three terms in equation (1.7):

$$O(\lambda) + O(\lambda) + O(\lambda^5) = 0 \tag{1.8}$$

This explains why the observed CP asymmetries in K decays, related to the tiny angle, are very small ($\sim 10^{-3}$).

On the other hand, the B meson system is related to the following equation:

$$V_{ud}V_{ub}^* + V_{cd}V_{cb}^* + V_{td}V_{tb}^* = 0 \tag{1.9}$$

where all the three terms are the same order of magnitude, $O(\lambda^3)$. This implies that all the three angle can be large in the triangle related to Equation (1.9), which leads to the possibility of large observable CP asymmetries in the B meson decays. The triangle related to B meson system (illustrated in Fig. 1.1) is sometimes called as *the* "Unitary Triangle".

Since only two generations are related to tree diagrams of the K meson decays, the sensitivity to the parameters related to the CP violation is limited in the K system. In B meson system, all the angle ϕ_1, ϕ_2 and ϕ_3 can be measured independently, which leads to precise tests of the Standard Model.

1.3 Measuring CP Asymmetry in B Meson Decays

B meson can be produced in two energy regions, a center-of-mass energy equal to the Υ(4S) mass or higher center-of-mass energy.

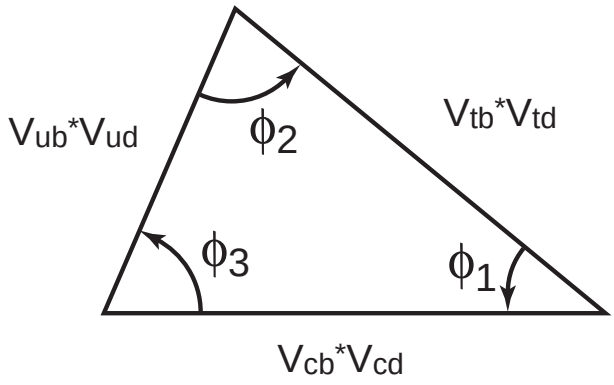


Figure 1.1: The Unitary Triangle

There are some advantages of producing B mesons at the Υ(4S) energy region. The $B\overline{B}$ cross section is higher than center of mass energy. $B-\overline{B}$ pairs are exclusively produced (50% $B^0\overline{B}^0$ and 50% B^+B^-). The energy of the produced B meson is known, which can be used to reduce the combinatorial background.

One of the most promising methods to measure CP angles in the B meson system is based on neutral B decays to CP eigenstates f_{CP} which are common to B^0 and $\overline{B}^0$. B^0 and $\overline{B}^0$ can "mix" through the loop diagrams shown in Fig. **??**. i.e. after a certain time, a meson which was B^0 at production will not be a pure B^0 state, but a mixed state of B^0 and $\overline{B}^0$. CP violation is induced by $B^0-\overline{B}^0$ mixing through the interference of the two decay amplitudes of B^0, $A(B^0\to f_{CP})$ and $A(B^0\to\overline{B}^0\to f_{CP})$. In order to detect this CP violation, one must know, or *tag* the flavor of the particle (B^0 or $\overline{B}^0$) at a given time.

On the Υ(4S), tagging one B as a B^0 or a $\overline{B}^0$ identifies the other with certainty. Since both C and P eigenvalues of Υ(4S) is -1 and the decay of Υ(4S) is caused by strong interaction which conserves CP, produced $B-\overline{B}$ should be in a CP eigenstate with eigenvalue of 1. Because spin of Υ(4S) is 1 and that of B is 0, B^0 and $\overline{B}^0$ mesons are produced with the orbital angular momentum of 1, which means the P eigenvalue of $B-\overline{B}$ system is -1. This restricts the C eigenvalue to be -1 and a $B\overline{B}$ pair will remain in a coherent $B\overline{B}$ state as long as neither B has decayed. If one of them is detected to be $B^0(\overline{B}^0)$ at a moment, the other is inevitably $\overline{B}^0(B^0)$ at that time. This is extremely important for measuring CP violation.

For example, consider one B^0 from Υ(4S) decays into semi-leptonic mode, like $B\to D^*l\nu$ ($l=e$ or μ), after t_1 from its production. If that particle was $B^0(=\overline{b}d)$ at t_1, the charge of lepton is positive (see Fig.??) and if it was $\overline{B}^0(=b\overline{d})$, the charge of lepton is negative. Thus one can tag the flavor of B mesons by detecting leptons from $B_{\rm S}$.

When the $B^0-\overline{B}^0$ pair is produced with odd relative angular momentum,

the rate for one of the neutral B mesons to decay as $\overline{B}^0$ at $t = t_1$ and the other (which is B^0 at $t = t_1$) to decay into CP eigenstate, for example $J/\psi K_S$, at $t = t_2$ is written as

$$P(B^0 \to J/\psi K_S; \Delta t) = \frac{1}{2} e^{-\Gamma|\Delta t|}(1 + \lambda \sin \Delta m \Delta t) \tag{1.10}$$

where Γ is the B meson total decay width, $\Delta t \equiv t_2 - t_1$, Δm is the mass difference between the two neutral B weak eigenstates and λ is the CP asymmetry parameter

$$\lambda = -\sin(2\phi_1). \tag{1.11}$$

The CP conjugate of this function is

$$P(\overline{B^0} \to J/\psi K_S; \Delta t) = \frac{1}{2} e^{-\Gamma|\Delta t|}(1 - \lambda \sin \Delta m \Delta t). \tag{1.12}$$

The Δt value ranges are from $-\infty$ to ∞ and it is easily seen that CP asymmetry vanishes in the time integrated rate. Therefore, the measurement of decay time difference, Δt is required to observe CP asymmetry in experiments at the Υ(4S).

In the normal colliders with symmetric energy, the Υ(4S) is produced at rest, consequently the B mesons are produced at rest. Momenta of $B_{\rm S}$ from Υ(4S) are about 325 MeV/c and the average decay length of the $B_{\rm S}$ is about 30 μm, if the Υ(4S) is produced at rest. Any time dependence measurement is impossible with the present vertex detectors for such a case.

A solution is to produce the Υ(4S) moving in the laboratory frame. This can be achieved by colliding two beams of unequal energy. This results in two B mesons boosted in the same direction along the beam axis. The average distance between the two B decay is approximately $\beta\gamma c\tau$ where $\beta\gamma$ is the boost parameter of the center of mass and τ is the average B lifetime. Since the B mesons move almost parallel to the beam axis, the decay time difference of two B mesons can be approximately calculated as

$$\Delta t \simeq \Delta z / \beta\gamma c \tag{1.13}$$

where Δz is the distance of the decay vertices along the beam axis. A precise measurement of the decay vertices of B mesons is necessary to measure CP violation in this scheme.

1.4 KEKB Accelerator

As described in the previous section, to measure CP asymmetry in decays of B mesons, one must produce Υ(4S) boosted in the laboratory frame. The KEKB accelerator [8] was designed to realize this. It has two rings in a tunnel which was used for TRISTAN, one for the electron beam and the other for the positron beam. The circumference of main rings are about 3 km. The configuration of the KEKB accelerator is shown in Fig. 1.2.

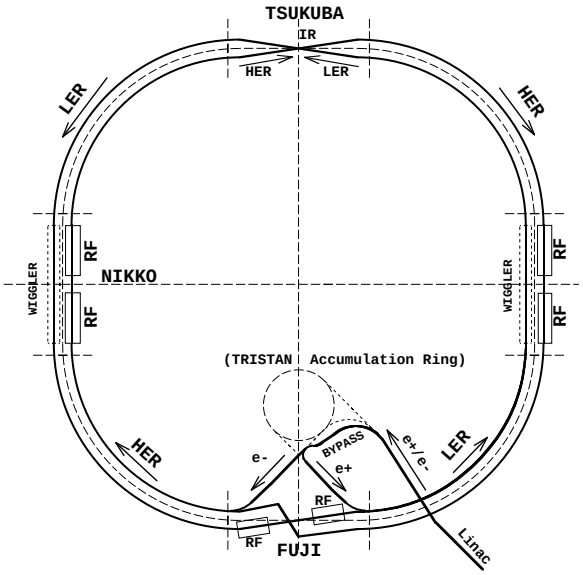


Figure 1.2: Configuration of the KEKB accelerator system

Beam energies are chosen to be $8GeV/c^2$ for electron and $3.5GeV/c^2$ for the positron, so that the center of mass energy comes on the $\Upsilon(4S)$ resonance. In such configuration, $\beta\gamma \simeq 0.425$ and the average decay length of B mesons from $\Upsilon(4S)$ is about 200μm in the laboratory frame.

In order to produce as much B mesons as possible, KEKB accelerator is designed to run at the highest luminosity in the world, 10^{34} cm^{-2}s^{-1}, corresponding to 10^8 of $B\overline{B}$ pairs in a year. As of the end of 2002, KEKB has achieved a peak luminosity of 8.3×10^{33}cm^{-2}s^{-1}.

1.5 Belle Detector

The Belle detector (Fig. 1.3) is a 4π detector designed for the study of CP violation in B meson system [9, 10]. The Belle detector consists of Central Drift Chamber (CDC), Aerogel Cherencov Counter (ACC) and Time of Flight counter (TOF), CsI calorimeter (ECL), K_L and Muon detector (KLM), and Silicon Vertex Detector (SVD).

As is described in the previous sections, precise vertex measurement and flavor tagging of B mesons are required for the study of CP violation. There are a number of candidates for the vertex detector, e.g. scintillating fiber, gas microstrip detector, etc. We decided to use double-sided silicon microstrip detector as vertex detector in the Belle experiment. The intrinsic resolution

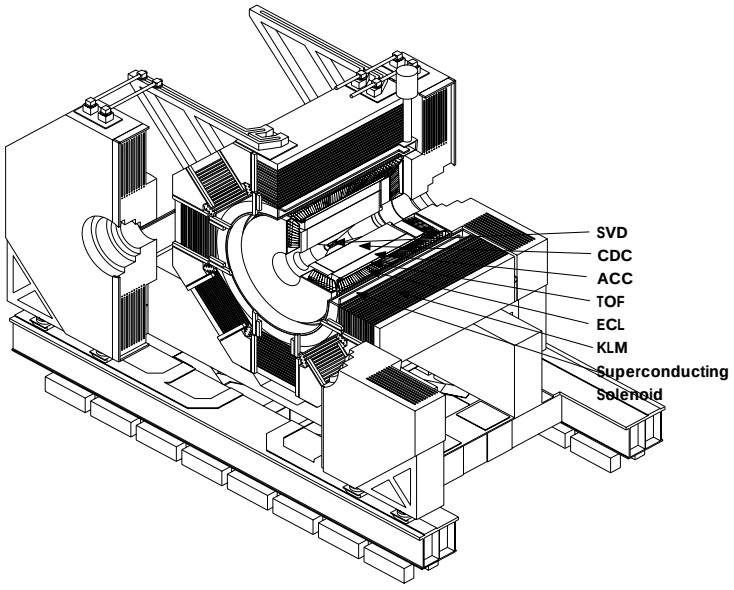


Figure 1.3: Schematic view of the Belle detector

order of 10μm can be achieved by the silicon strip detector. The effect of multiple scattering, which is of great importance in the Belle momentum region (typically $p \sim 1$ GeV), is minimized by use of double-sided silicon strip detector.

The flavor of B meson which decays into CP eigenstate (B_{CP}) is determined by the flavor of the other B meson (B_{tag}). There are mainly two methods to tag the flavor of B. One method is based on semileptonic B decays. The charge of leptons (e and μ) indicates the flavor of the B. The charge of kaon also indicates the flavor of the B, since $b \to c \to s$ decay chain is dominant process. Good K/π separation is required for the kaon tagging.

In the Belle, electrons are identified by the CDC and ECL. Muons are detected by the KLM. The CDC, TOF and ACC provide K/π separations up to $3.5GeV/c$. The CDC covers the momentum up to $0.8GeV/c$, the TOF covers up to $1.2GeV/c$ and the ACC covers momentum range $1.2 < p < 3.5GeV/c$.

Charged tracks are primarily reconstructed by the CDC. Photons are detected by the ECL. K_L's are detected by the KLM.

1.6 Goal of this Study

As described in Sec.1.3, it is important to measure the distance of the projection of the decay distance of two B mesons (Δz) precisely. We have used Silicon Vertex Detector (SVD) as a high resolution position detector.

The performance of the current SVD is satisfactory, its design leaves room

for improvement. Therefore we have worked in order to upgrade SVD. Major upgraded point are as follows:

1. Radiation tolerant (20 MRad) readout chip (VA1TA).
2. Larger angular acceptance.
3. Increase the number of layers from 3 to 4 .
4. Smaller radius of inner-most layer (3.0 cm $\rightarrow$2.0 cm).

Goal of this study is to construct the upgraded SVD and to check its performance. The outline of this thesis is as follows:
In Chapter 2, we describe the design of the upgraded SVD. The assembly procedure of the ladder is described in Chapter 3. The result of performance test using real detector system is presented in Chapter 4. Finally, we conclude this thesis in Chapter 5.

Chapter 2

Upgraded SVD

In this chapter, we describe the design of upgraded SVD (SVD2), after briefly describing the current SVD (SVD1).

2.1 SVD1

2.1.1 Overview

The main task of the Silicon Vertex Detector (SVD) [11] is to reconstruct the decay vertices of two primary B mesons in order to determine the time difference between two decays. The SVD is designed so that its intrinsic resolution is expected to be a few tens of μm, which is much better than the resolution of a wire drift chamber.

The Belle SVD is set just inside the CDC and reconstructs precise tracks of charged particles combining the CDC measurement. The CDC can reconstruct low momentum tracks down to p_T of about 70 MeV/c since inner radius of the CDC is about 8 cm. The SVD is not required to function as a stand-alone tracker for low p_T tracks.

Multiple-Coulomb scattering is a dominant source of the vertex resolution degradation. This imposes strict constraints on the detector design and the mechanical layout. The innermost layer of the support structure must be low mass but stiff; and the readout electronics must be placed outside of the tracking volume.

2.1.2 Detector Configuration

The SVD has three cylindrical layers consisting of units of the silicon sensors. The position of each layer is 3.0 cm, 4.55 cm and 6.05 cm in r direction, respectively. The SVD covers $23° < \theta < 139°$, corresponding to the angular acceptance of 86 %. The three layers have 8, 10 and 14 sensor modules (ladders) in ϕ. The structure of the SVD is shown in Fig.2.1. Each layer is constructed from double-sided silicon strip detectors (DSSDs) and the front end electronics.

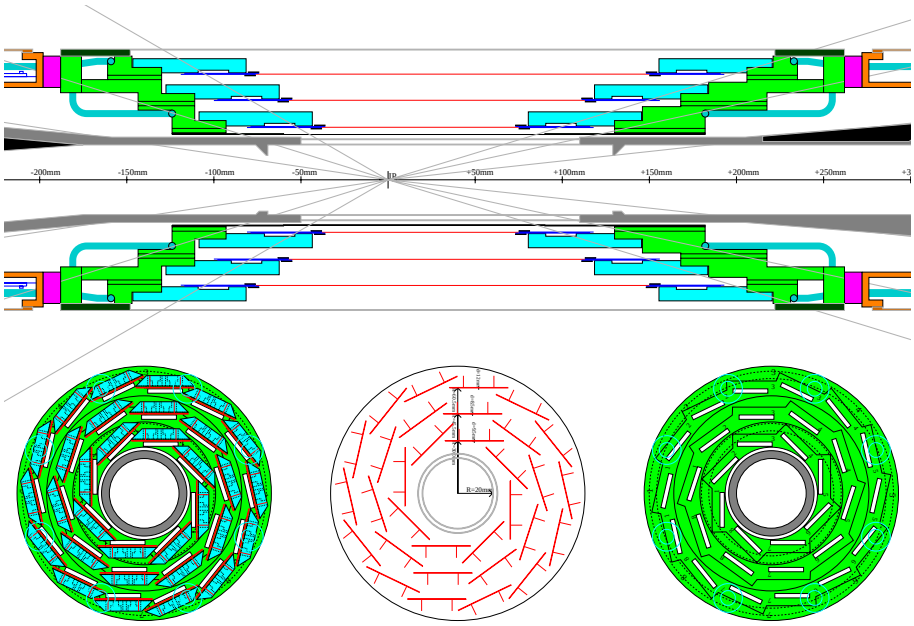


Figure 2.1: Configuration of SVD1

DSSD The one side (= n-side) of the DSSD has n^+-strips oriented perpendicular to the beam direction to measure the z coordinate. The other side (= p-side) with longitudinal p^+-stripes allows ϕ coordinate measurement. The z strip pitch is 42 μm and the ϕ strip pitch is 25 μm. The bias voltage of 75 V is supplied to the n-side and p-side is grounded. P-strips and n-strips detect electron-hole pairs which are induced by charged tracks.

Readout System The signals from DSSD are read out by VA1 chip mounted on hybrid board and transferred via thin cables to a buffer card (ABC) followed by thicker cables and a repeater board (REBO). Flash ADC (FADC) modules are installed to digitize the analog signal and send the digitized signal to the central DAQ system.

VA1 chip The VA1 [12] is 128 channel CMOS integrated circuit designed for the readout of silicon vertex detectors and other small signal devices. The VA1 is radiation tolerant to levels of order 200 kRad [13].

CORE (COntrol and REpeater) system Repeater system [14] consists of small cards near the detector (ABCs), boards for signal buffering and fronted control (REBO), a board for monitoring (RAMBO), a mother board (MAMBO) and their cooling shielding case (DOCK).

Signals from a side of DSSD are read by five VA chips on a hybrid board and sent to repeater system. Two cables from two hybrid boards are merged on an ABC. The flat cable is connected to a MAMBO contained in a DOCK. A MAMBO has five slots.

Signals from ABC are sent to REBO through a local bus. After amplification and filtering, differential signals are sent to back-end electronics system located in the electronics hut. All the timing and control signals, bias voltages and power supplies from backward electronics are fed to MAMBO and then distributed to each board or sent to front-end electronics.

2.2 Upgrade of SVD

We plan to upgrade the Vertex Detector, SVD1 to SVD2 in the summer 2003. Major upgraded point are as follows:

1. Radiation tolerant (20 MRad) readout chip (VA1TA).
2. Larger angular acceptance.
3. Increase the number of layers from 3 to 4 .
4. Smaller radius of inner-most layer (3.0 cm $\rightarrow$2.0 cm).
5. Floating ground.

2.2.1 Radiation Tolerance

Radiation tolerance is one of the most significant improvement of SVD2. The KEK B-factory achieved the highest luminosity in the world, and it provides the potential for many precise measurements. On the other hand, under the high luminosity operation, the detectors near the beam line suffer very high radiation. In SVD1, the radiation damage causes the gain drop of VA1 chip, and it increases the noise level due to the leakage current of DSSDs. Although the front-end IC, the VA1, remains functional to 200 kRad (1 MRad after the second replacement in 2000), it exhibits a significant increase in noise at lower levels. Moreover, the 200-kRad level affords almost no margin for error in accelerator and detector operations. In the present status, radiation dose is a few hundred kRad per a year. We have already exchanged SVD two times because of the radiation damage. Therefore radiation tolerant SVD has been desired.

2.2.2 Geometrical Improvement

Larger angular acceptance is another improvement of SVD2. SVD1 covers the polar angle range $23^\circ < \theta < 139^\circ$ while the CDC angular coverage is $17^\circ < \theta < 150^\circ$. The effect of this reduced coverage is not limited to the loss of vertexing capability. Since the support material for the SVD ladder is in the tracking volume of the CDC, it degrades the performance of both charged and neutral particle tracking. SVD2 covers the same angular range as the CDC ($17^\circ < \theta < 150^\circ$).

The relatively small radius of the innermost layer is another improvement. SVD1 uses a commercially available double-sided strip detector (DSSD), the S6936, which was originally developed for the DELPHI experiment at CERN. Due to the width of these DSSDs and the requirement of the overlap for alignment, the minimum radius was 3.0 cm. To improve the impact parameter resolution, a smaller radius is highly desirable. Therefore we set the radius of the innermost layer of SVD2 to be 2.0 cm. In SVD2, we also increase the number of the layers from 3 to 4. We expect these improvement to lead to the impracement of the impact-parameter by 30 %.

2.2.3 Floating Ground

Floating ground is another improvement. Failure of the integrated AC-coupling capacitors in the DSSDs is a serious problem in SVD1. We call this problem "pin-hole". It is a dominant source of the loss of strip yield (about 3 %) and detector yield. Moreover, the potential for losing additional strips persists even after detector installation. In each system installation, pin hole occurred at a rate of 2$\sim$3 half-ladder per a year. If this problems happens after detector installation, we can't set this half-ladder sufficient bias voltage due to large leakage current. Therefore, we can't use a whole half-ladder as a detector. This is very serious problem.

Floating ground of SVD2 can solve this problem. In SVD2, ground level of front-end IC is set to almost the same level as DSSD bias. Even if a pin-hole occurs, we can apply enough detector bias voltage because the voltage difference between the strips and front-end ICs is a few volt and the leakage current is small.

2.3 SVD2

2.3.1 Detector Configuration

Taking into account the considerations above, we reached the following baseline design for the upgrade, SVD2. Figs. 2.2 and 2.3 show the side and r-ϕ view of SVD2.

SVD2 consists of four layers of DSSD ladders and covers the angular range $17^\circ < \theta < 150^\circ$. The innermost layer has a radius of r = 2 cm, while the outermost layer rests at r = 8.8 cm (see table.2.1. All ladders in layer 1, 2, and 3 are constructed from identical DSSDs. The DSSDs are connected to the front-end ICs via a flex circuit. The flex circuit also serves to fan out the signals from z -strips, eliminating the need for double-metal readout on the DSSD. Use of a flex circuit also allows the DSSDs to be placed closer to the interaction point, independent of support structure.

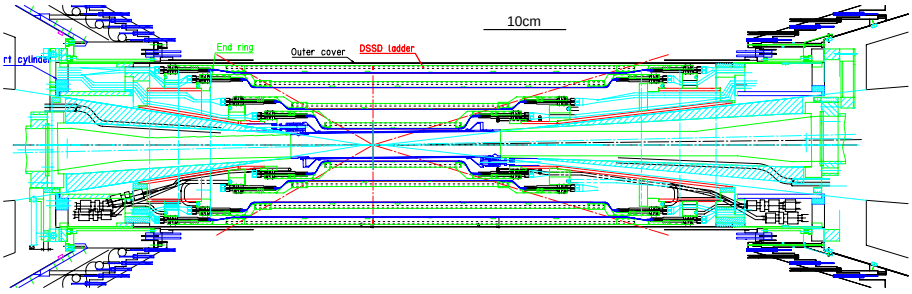


Figure 2.2: Side view of SVD2

Table 2.1: Inner radius, number of ladders in each layer.

Layer	r (mm)	number of ladders
1	20.0	6
2	43.5	12
3	70.0	18
4	88.0	18

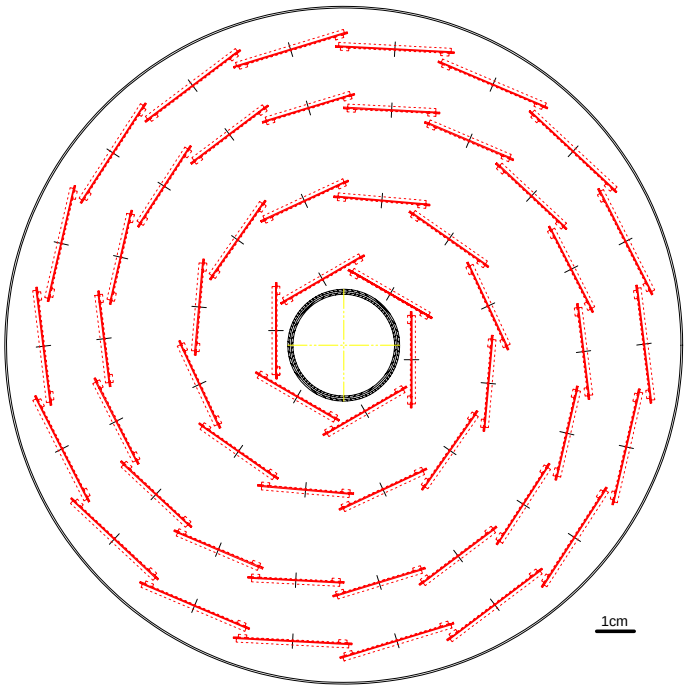


Figure 2.3: r-ϕ view of SVD2

Table 2.2: Number of DSSD for a ladder and half-ladder in each layer

Layer	N_z	Forward-side	Backward-side
1	2	1	1
2	3	1	2
3	5	2	3
4	6	3	3

2.3.2 Mechanical Structure

The mechanical structure of SVD2 consists of four layers of DSSD ladders, end rings, support cylinders, and an outer cover as shown in Figs.2.2 and 2.3. The forward and backward support cylinders are connected by the outer cover, and they form the basic mechanical structure of SVD. The DSSD ladders are mounted on the forward and backward end rings, which are supported by the forward and the backward support cylinders. The support cylinders are in turn supported by the CDC end plates. The precision of the machining and assembly is better than 50 μm. The beam pipe is also supported by the CDC end plates. The beam pipe support is designed such that the heat load and any vibrations originating from the pipe and its cooling system should not affect the performance of the SVD system.

2.3.3 DSSD

Two types of DSSDs are fabricated for SVD2. We minimize the number of types of DSSD to simplify bookkeeping and ladder assembly. In particular, in layers 1, 2 and 3, the same sensor is used for all ladders. The number of DSSD used in each layer is shown in table.2.2.

Wider DSSDs are used in the outermost layer so that total number of ladders can be kept less than 30. This constraint comes from the available number of readout channels in the repeater system. We chose $2.56 \times 7.68\text{cm}^2$ and $3.33 \times 7.38\text{cm}^2$ for the active DSSD size for the inner 3-layers (layers 1, 2 and 3) and the outermost layer, respectively. The length of the outermost DSSD is limited by the size of the wafer (4 inches).

The DSSDs for the inner 3-layers consist of 512 ϕ-strips with 50 μm pitch and 1024 z-strips with 75 μm pitch. The DSSDs for the outermost layer consist of 512 ϕ-strips with 65 μm pitch and 1024 z-strips with 73 μm pitch. Every ϕ-strip for each layer DSSD is connected to a preamplifer channel. On the other hand, every second z-strip is connected to a preamplifer channel. Flex circuits are used instead of double-metal structure to read out the z -strips so as to minimize the capacitance due to the overlap of readout traces and strips. A small overlap capacitance is important to minimize the charge loss from the capacitive charge division. Polysilicon resistors are implemented to bias each strip.

The ohmic side is used to measure the ϕ -coordinate while the junction side provides a z measurement. This arrangement allows us to balance the capacitance between the ohmic and junction sides. The ohmic side and the z -measurement sides tend to have larger capacitance due to their more complex structure. An "atoll" type p-stop structure is employed on the ohmic side to minimize p-stop noise.

We implement integrated AC-coupling capacitors. However, all strips, including strips with broken capacitors, are connected to preamplifers to take advantage of the DC capability of the preamplifer. This arrangement increases both the strip yield and the detector yield while protecting most of the preamplifer channels from accidents. This also eliminates concerns regarding post-installation breakdown of the AC-coupling capacitors.

Tables 2.3, 2.4 and 2.5 summarize the specifications for the DSSD.

Table 2.3: Specifications common for all types of DSSDs

Parameter	Junction side	Ohmic side
Thickness	300 μm	
Readout(Bias) method	AC(Poly-Si)	
Full depletion voltage (V_{fd})	80 V Max	
Breakdown voltage	100 V Min	
Leakage current at V_{fd}	5 μA	
Bias resistance	100 MΩ typ.	
Passivation	SiO_2	

Table 2.4: Specifications for DSSDs of layer 1, 2, and 3

Parameter	Junction side	Ohmic side
Chip size	79.2 mm $\times$ 28.4 mm	
Active Area	76.8 mm $\times$ 25.6 mm	
Strip pitch	75 μm	50 μm
Number of strips	1024	512
Strip width	50 μm	12 μm
Readout electrode width	56 μm	10 μm

2.3.4 Flex Circuits

In contrast to SVD1, where the silicon sensors were wire-bonded directly to the VA1 readout chips, SVD2 uses a flexible printed circuit board (flex) to connect the silicon sensors and the readout chips. Wire-bonding is done between DSSD

Table 2.5: Specifications for DSSDs of layer 4

Parameter	Junction side	Ohmic side
Chip size	76.4 mm × 34.9 mm	
Active Area	73.8 mm × 33.3 mm	
Strip pitch	73 μm	65 μm
Number of strips	1024	512
Strip width	55 μm	12 μm
Readout electrode width	61 μm	10 μm

and flex, flex and VA1TA chip. Figs.2.4 and 2.5 show the flex circuit used for z-side of layer-4. The circuit is made on a film of the Kapton. The thickness of the film is 50 μm. All the circuit lines and elements are on one side of the film with nothing on the other side. The trace material is gold-plated copper. The thickness of the line is about 5 μm. Flex Circuits are produced by Keycom company in Japan.

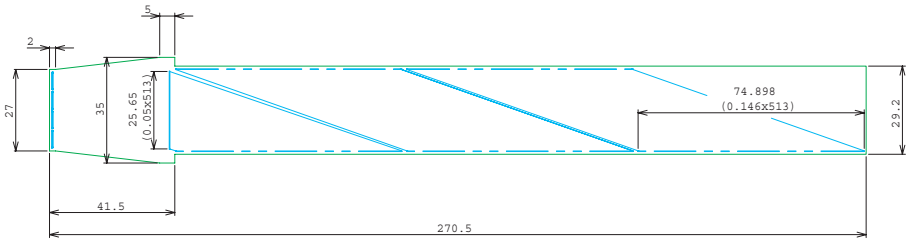


Figure 2.4: Flex circuit (for layer-4 z-side)

2.3.5 Readout System

Fig.2.6 shows a block diagram of the overall readout system. The system is physically distributed over three sites: (i) VA1TA chips mounted hybrids located in close proximity to the DSSDs; (ii) a repeater system, also called the "CORE" system, located just outside the final quadrupoles about 2 m from the IP; and (iii) the FADC, DAQ, and trigger boards located in the electronics hut, which is an approximately 35m cable run from the detector.

VA1TA chip

Fig.2.7 shows a picture of the VA1TA chip. The VA1TA is a 128-channel preamplifier-shaper integrated circuit, with simultaneous sample and hold, multiplexed analog readout and calibration facilities. Each channel has a preamplifier, a slow shaping time amplifier (slow shaper), a fast shaping time amplifier

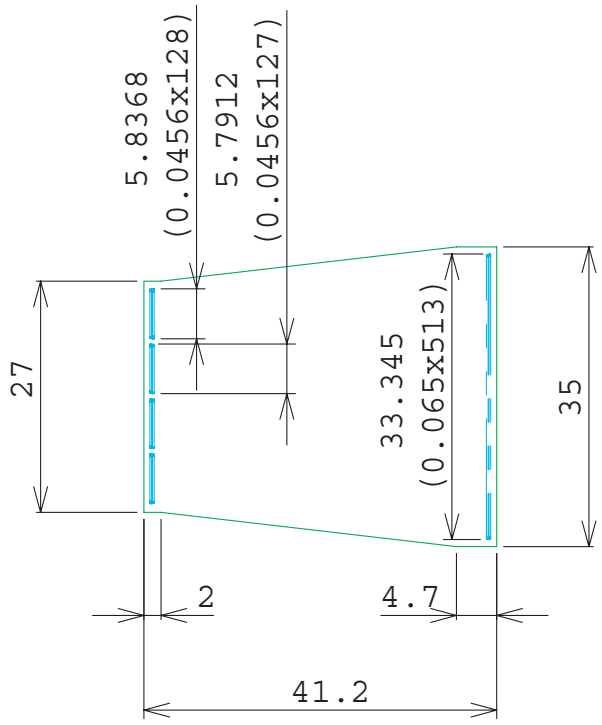


Figure 2.5: Flex circuit (for layer-4 ϕ-side)

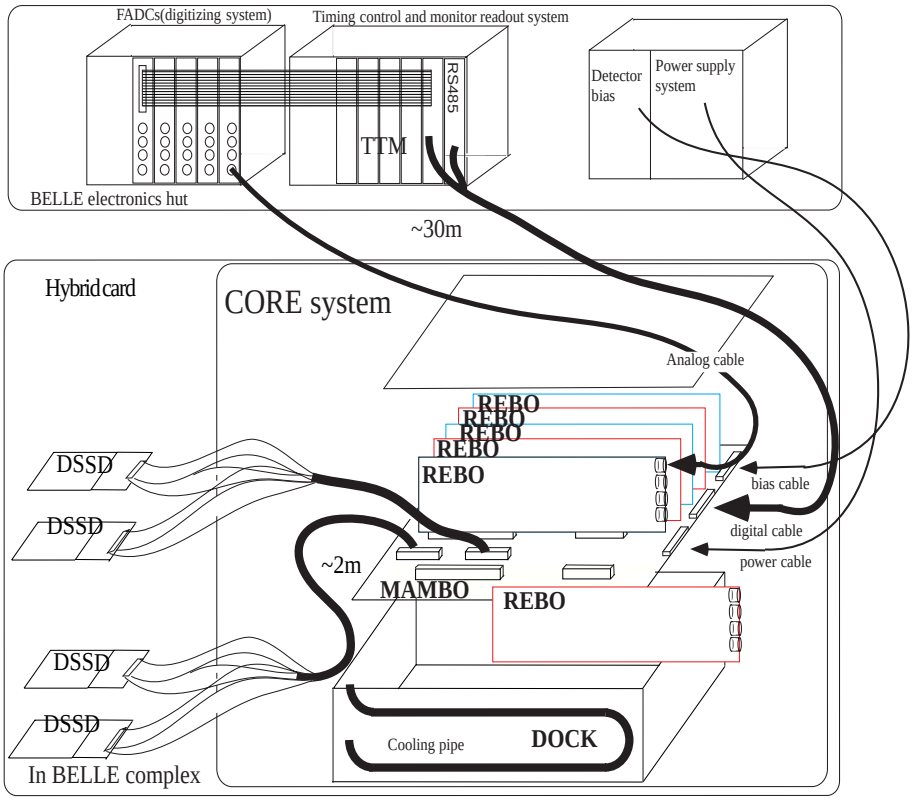


Figure 2.6: Block diagram of the SVD2 readout system

(fast shaper), a discriminator and a monostable multivibrator. All biases are generated internally from the externally applied current bias and can be adjusted by on-chip DACs. The VA1TA provides testing inputs of the individual channels. The gain of the VA1TA can be calibrated by the test pulses.

The VA1TA is fabricated with the AMS 0.35 μm process. It is known that the radiation hardness scales as the cube of the feature size of the process in the deep sub-micron region. The VA1 with the AMS 0.35 μm process is measured for the radiation hardness to be over 20 MRad [15].

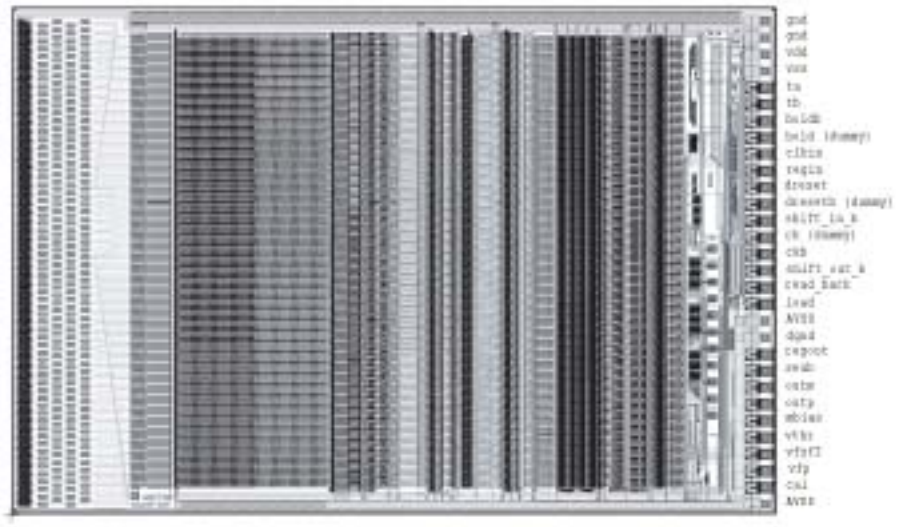


Figure 2.7: Picture of the VA1TA chip

Fig.2.8 shows the principle of VA-TA. TA and VA share the same preamplifier which is located on the VA. The inputs of TA is directly coupled to corresponding outputs of these preamplifiers.

Fig.2.9 shows the readout timing of VA1TA. After the physics event, each channel integrates the signal. Then an external hold signal (holdb) is applied to sample the analog value. The peaking time of shaper is typically set to 500 ns. Immediately after this a sequential readout can be performed by activating the output bit-resister using "shift_in_b" and clock signal (ckb).

Hybrid

The hybrid is a board for readout on which 4 VA1TA chips are mounted. Two single-sided hybrids are glued back-to-back to form a hybrid pair unit. A copper plate is sandwiched between two hybrids as a heat conductor. Fig.2.10 shows

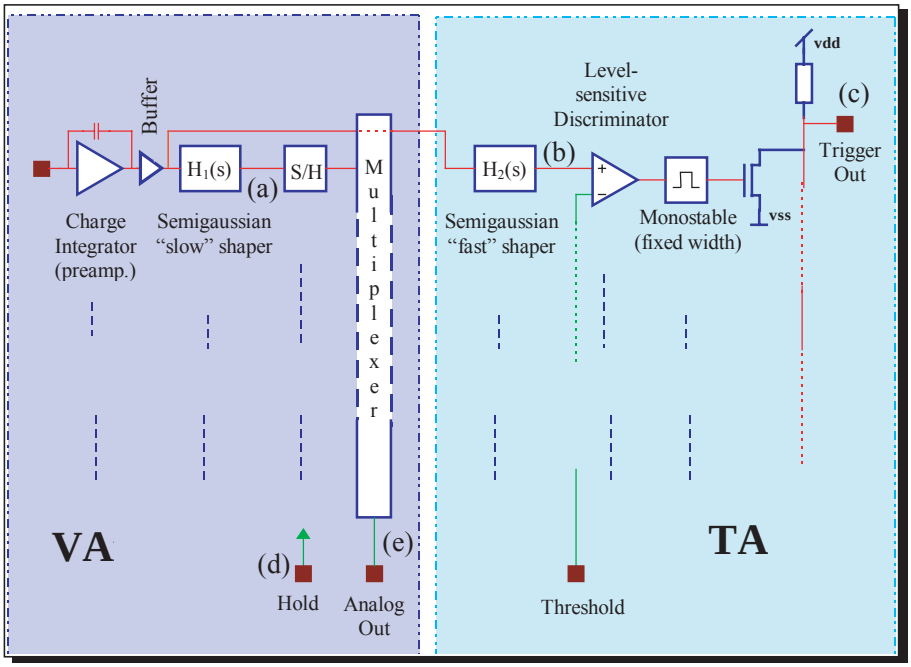


Figure 2.8: VA1TA principle

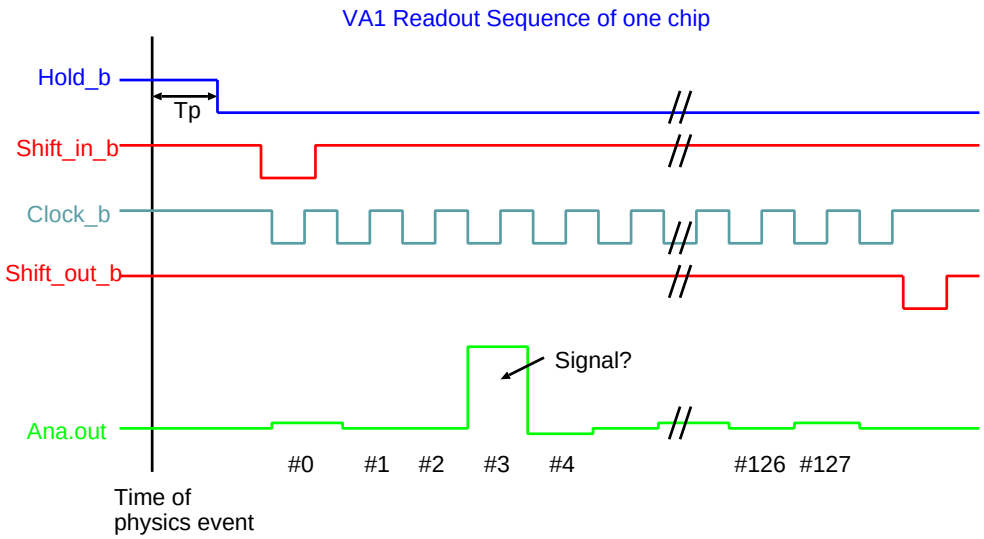


Figure 2.9: Readout sequence of VA1TA

a picture of a hybrid board. The circuitry is printed on a multilayer aluminum nitride (AlN) substrate produced by the Kyocera company in Japan.

Since preamplifier chips are heat source, we paid careful attention to the thermal path way through the hybrid, across glue joints, copper plate, AlN base.

In contrast to the hybrid of SVD1, with which five VA1 chips are serially read out, four VA1TA chips of the hybrid of SVD2 are read out in parallel. This enables us to reduce the time to read out and reduce the dead time.

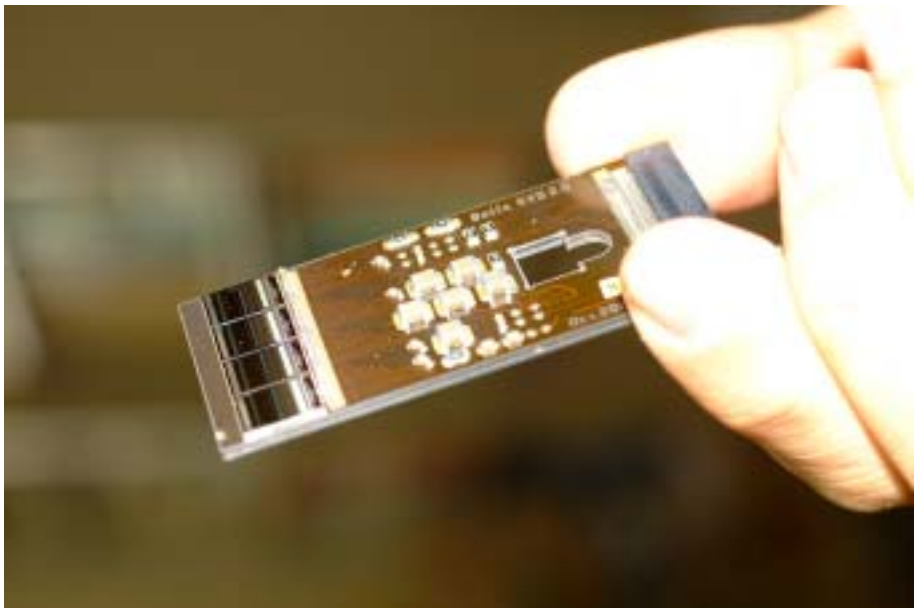


Figure 2.10: Picture of the hybrid

Back-end Electronics

Here, we briefly describe back-end electronics (see Fig.2.6).

The repeater system provides full control of the SVD front-end electronics and takes care of the analog signals from multiplexers on the VA1TA chips on the hybrids to the FADCs in the electronics hut. The repeater system also distributes the detector bias and hybrid power-supply voltages.

The system comprises two boards design: a motherboard (MAMBO) and a repeater board (REBO). Each of the ten repeater docks consists of six identical

REBOs plugged into a single MAMBO. Three of the REBOs in each dock are used for positive-bias detectors and the other three are used for negative-bias detectors. The MAMBOs handle the distribution of positive and negative detector bias voltages. The MAMBOs also receive and distribute control signals from the off-detector electronics.

Overall steering of the fast trigger and control signals is done using trigger-timing modules (TTMs) housed in the electronics hut. The REBO also receive and retransmit analog signals from the front-end hybrids (four hybrids per REBO) and implement the DC level shift needed because of the floating ground scheme. The level-shift will be accomplished using either analog opto-couplers or by AC coupling with a DC baseline restoration circuit. The REBOs also monitor the shift-out signal from hybrids, which is a good check on the proper operation of the VA1s.

Analog signals from REBOs are sent to FADCs. We use thirty-six FADCs to process the signals. FADC modules are installed to digitize the analog signal and send the digitized signal to the central DAQ system.

Chapter 3

Ladder Assembly

3.1 Overview

We call assembled module of SVD "ladder" (shown in Fig.3.1). In this chapter, we explain the procedure of ladder assembly. Fig.3.2 shows a schematics of a layer-3 ladder (ladders for other layers are almost identical, although the number of DSSDs is different).

Each ladder consists from two electrically independent "half-ladders". A half-ladder is made of DSSDs, hybrids, and flex circuit. A full-ladder consists of two half-ladders, bridges, AlN bases, and a support rib (ZYLON+CFRP).

The assembly procedure is as follows.

1. Gluing z-flex to DSSDs and hybrid pair.
2. Gluing ϕ-flex.
3. Wire bonding (DSSD-DSSD(ϕ-side), DSSD-flex(z-side), and flex-VA1TA).
4. Gluing two half-ladders, AlN bases, bridge, and support rib to full-ladders.

In this chapter, mainly we illustrate the assembly procedure of layer-4 ladder, but almost the same procedure is applied to the other layers.

3.2 Components of the Ladder

Fig.3.3 shows a side view of the full-ladder around a hybrid. In this section, we describe components other than DSSD, hybrid, and flex circuit.

3.2.1 AlN Base

Fig.3.4 is a schematic drawing of an AlN base. The base is set under the hybrid. The base is also used as a heat conductor.

Figure 3.1: Picture of the real ladders
From the bottom to the top, a ladder for layer-1, 2, 3, and 4,respectively

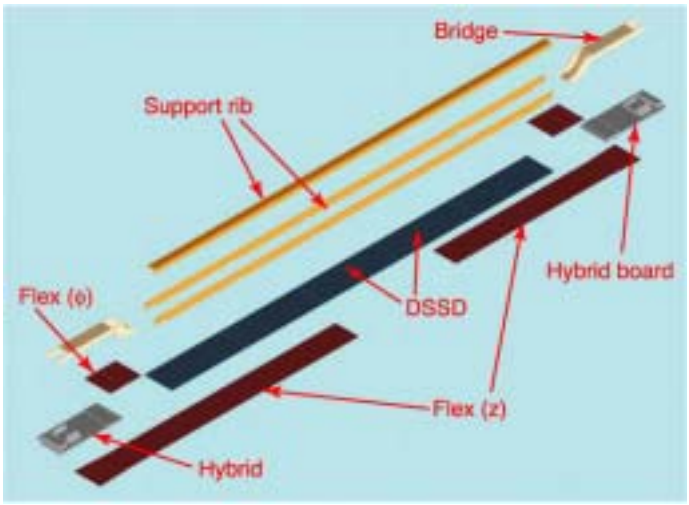


Figure 3.2: Schematics of the components of a ladder

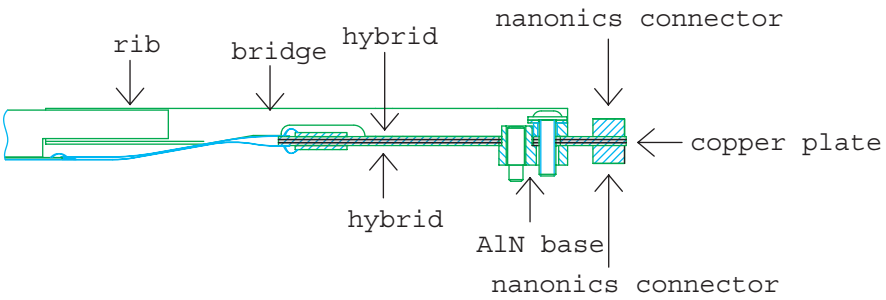


Figure 3.3: Side view of the ladder around hybrid

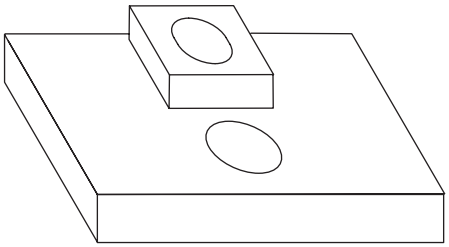


Figure 3.4: A schematic drawing of the AlN base

3.2.2 Bridge

A bridge is used to connect hybrid pair and support rib. A schematic drawing of the bridge is shown in Fig.3.5.

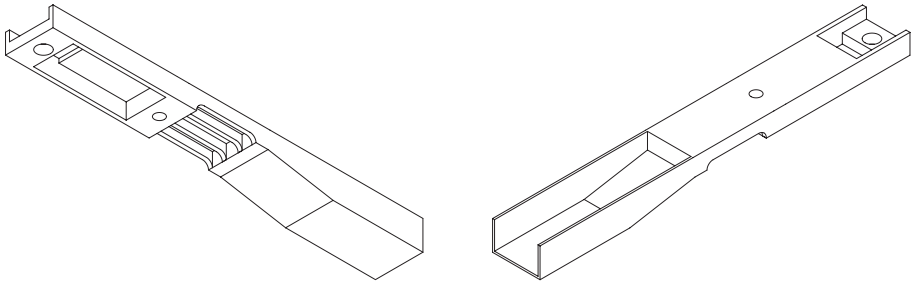


Figure 3.5: A schematic drawing of the bridge

3.2.3 Support Structure

To keep the strength of ladder, support rib is used. Fig.3.6 is a schematic drawing of the support rib. The rib consists of a CFRP roof and a ZYLON wall. In case of SVD1, support structure consists of BN (boron nitride) and CFRP. However, since SVD2 ladders are longer than SVD1 ones, so we have chosen ZYLON, so as to obtain enough support strength without increasing the material. ZYLON is new high-performance fiber developed by TOYOBO. ZYLON consists of rigid-rod chain molecules of poly (p-phenylene-2,6-benzobisoxazole)(PBO). Fig.3.7 shows the chemical structure of ZYLON.

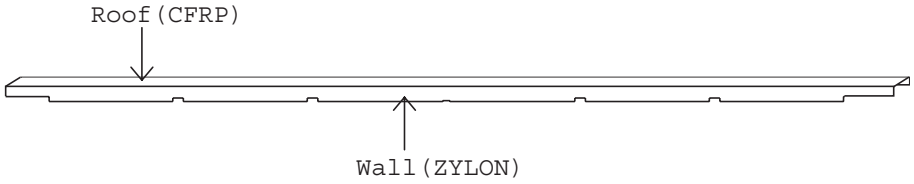


Figure 3.6: Support rib

Fig.3.8 shows support concept of SVD2 and SVD1. In case of SVD2, we apply a box structure (CFRP, ZYLON, and DSSD itself) which provides enough support strength without increasing material.

Figure 3.7: Chemical Structure of ZYLON

3.2.4 Contribution to the Ladder Thickness

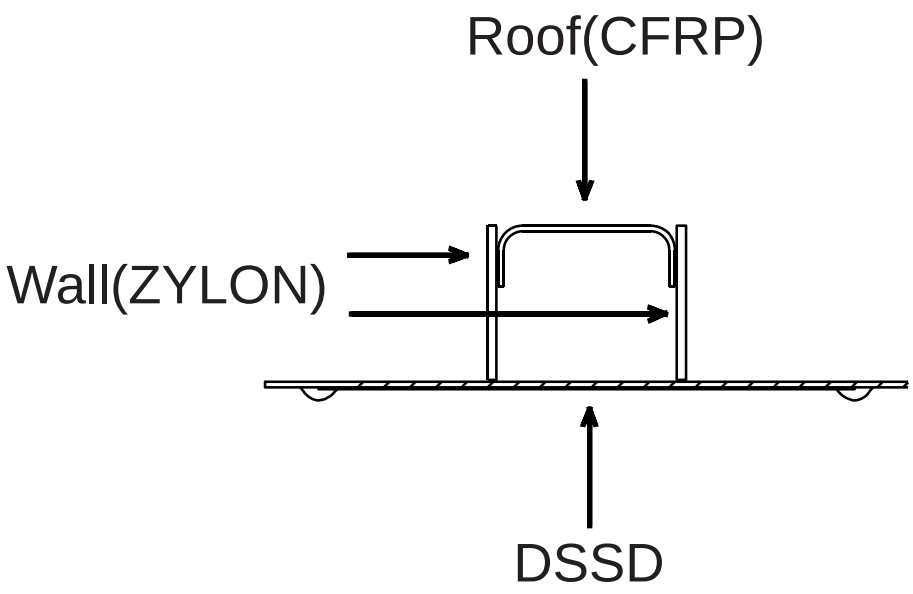
Table.3.2 and 3.3 show contribution to the ladder thickness of the support structure of SVD2 and SVD1 (see Fig.3.1 about physical parameter of material used for mechanical structure of a ladder). Even the length of the ladder is longer than the one of SVD1 (36 cm→62 cm in the outermost layer), the average material of a ladder (0.47 $\%X_0$/layer) is kept to be the same as SVD1.

Table 3.1: Material used for mechanical structure of a ladder

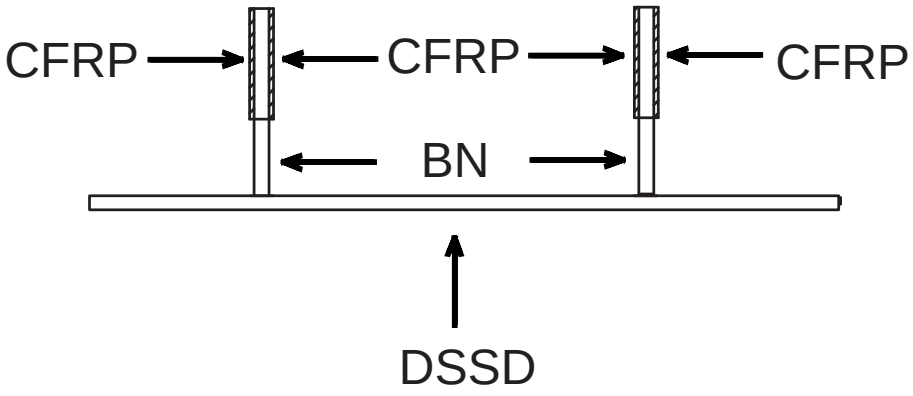
Component	amount of substance (g/cc)	Young's modulus (GPa)	Radiation Length (mm)
ZYLON	2.6	90	260
CFRP	1.7	170	240
DSSD (Si)	110	0.32	94

Table 3.2: Contribution to the amount of material per layer (SVD2)

Component	Thickness (mm)	Average material ($\%X_0$)
ZYLON	0.24	0.09
CFRP	0.14	0.06
DSSD (Si)	0.3	0.32
Total (support rib + DSSD)		0.47



(a) SVD2



(b) SVD1

Figure 3.8: Schematic views of the DSSD support for (a) SVD2 and (b) SVD1

Table 3.3: Contribution to the amount of material per layer (SVD1)

Component	Thickness (mm)	Average material ($\%X_0$)
CFRP+BN (boron nitride)	0.29	0.15
DSSD (Si)	0.3	0.32
Total (support rib + DSSD)		0.47

3.3 Half-ladder Assembly

In this section, we describe the procedure of half-ladder assembly.

3.3.1 Gluing z-flex

In the first step, z-flex is glued to the hybrid pair unit and DSSDs (Fig.3.9 shows a conceptual diagram).

We use two jigs. One is the jig which fixes z-flex (z-flex jig) shown in Fig.3.10 and another is to fix DSSDs and hybrid pair (DSSD/hybrid jig) shown in Fig.3.11.

To assemble the detector module precisely, hybrid pairs and DSSDs are glued with flex circuit, using alignment structures. In order to glue modules, we use the epoxy 'chiba-AW106' which was also used for SVD1.

Glue has to be applied to a flex in a controlled manner. A machine controlled syringe is used to regulate the amount of the glue and align the position. Z-flex is fixed by jig and applied glue as shown in Fig.3.10(red lines mean glue).

In this stage, it is very important to keep uniformity of glue under the flex circuit, because thickness and uniformity of glue under the flex circuit affects the easiness of the wire bonding significantly. Therefore we tune all parameters to keep the uniformity of glue; the speed of the syringe, the pressure to eject glue, and the distance between the nose of the syringe and the target can be controlled.

The alignment jig consists of an aluminum base, a Delrin bed, and vacuum chucks. The Delrin bed has a slight gap to set components precisely.

DSSDs, hybrid pair, and glass chip are placed on the Delrin bed, slid up against the alignment gap and fixed (see Fig.3.11). Next, two jigs are put on each other and these components were glued as shown in Fig.3.12.

When we developed the assembly procedure, we faced difficulty in the wire-bonding. Bonding pads of DSSD-flex have no solid ground. First, we filled this space with glue. But ununiformity of the thickness of glue and bubbles inside glue caused bonding failure. Therefore we introduced a "glass chip". Thickness of the glass chip is the same as DSSD (300 μm). The glass chip is set into the space between z- and ϕ-flex as a solid ground (Fig.3.9). This enabled us to wire-bond properly.

These components are held in the fixed position for 24 hours in order to

cure the epoxy. We keep the temperature of the assembly room around 23°C to guarantee the strength of the glue.

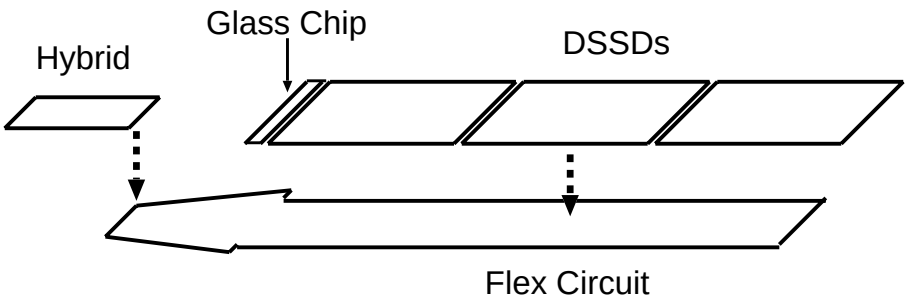


Figure 3.9: Conceptual diagram to glue z-flex to Hybrid and DSSDs

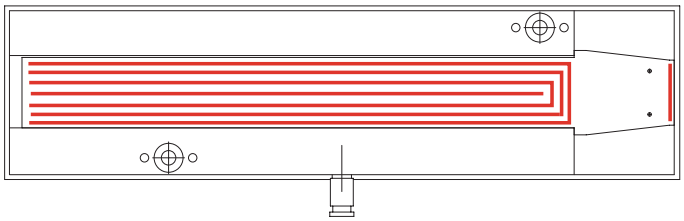


Figure 3.10: Z-flex jig and gluing position

3.3.2 Gluing ϕ-flex

In the next step, ϕ-flex is glued to the unit made in sec.3.3.1 (Fig.3.13 is a conceptual diagram). The procedure is similar to that described in Sec.3.3.1. Fig.3.15 shows the positon where we put glue (red lines). Φ-flex is fixed with ϕ-flex jig (Fig.3.14) and glued to DSSDs and hybrid pair as Fig.3.16)

In this stage, this unit is also fixed for 24 hours in order to cure the epoxy.

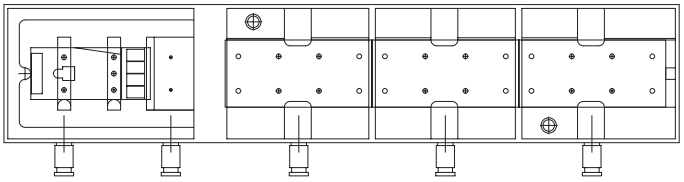


Figure 3.11: Jig to align and fix DSSDs and hybrid pair (DSSD/hybrid jig)

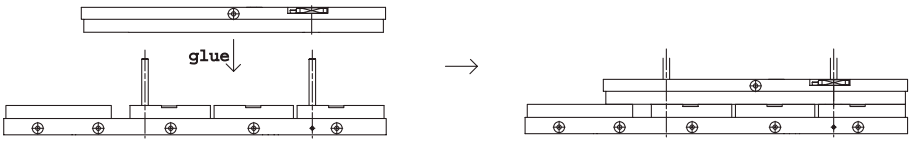


Figure 3.12: Gluing z-flex

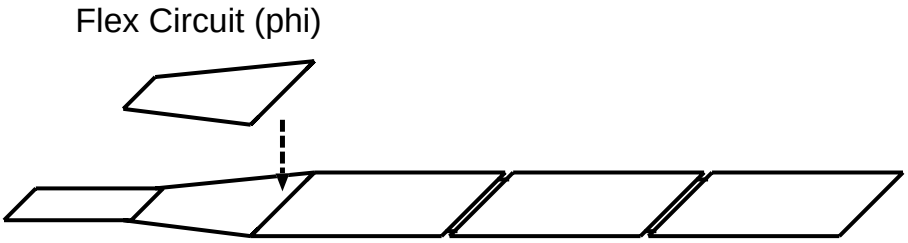


Figure 3.13: Conceptual diagram to glue ϕ-flex

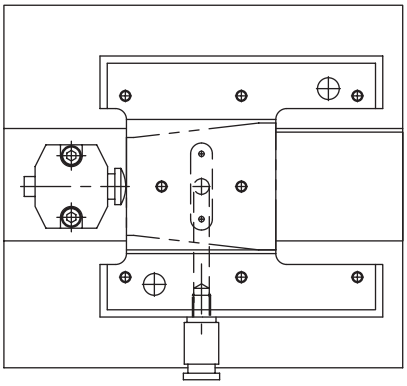


Figure 3.14: ϕ-flex jig

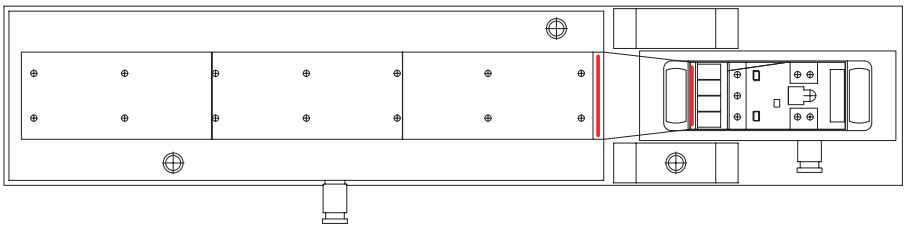


Figure 3.15: Gluing position(ϕ-flex)

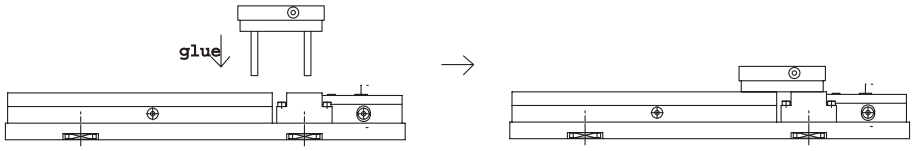


Figure 3.16: Gluing ϕ-flex

3.4 Wire Bonding

After half-ladder is assembled, wire bonding is done in order to electrically connect VA1TA chips to flex and flex to DSSD.

An automatic wire-bonding machine was operated by HPK technicians. Although bad strips were not wire-bonded in the case of SVD 1, all strips were wire-bonded this time.

Fixtures to hold half-ladder during wire-bonding were made so that after bonding one side, one could reverse the half-ladder to bond the other side.

Production rate is 1.5 half-ladder per a day.

3.5 Full-Ladder Assembly

After wire-bonding, half-ladders are assembled in pairs to form full-ladder. Two half-ladders are combined using epoxy to build a full-ladder.

Before two half-ladders are combined, a bridge and an AlN base are glued on the half-ladder (shown Fig.3.17). Next, two half-ladders are glued. Two half-ladders fixed to the jig are set to the base alignment fixture. Finally, a support rib is glued on two half-ladders (Fig.3.18). In this stage, this unit is also fixed for 24 hours in order to cure the epoxy.

The assembled ladders are mounted on the structure of SVD2 at KEK. Fig.3.19 is a picture of the completed SVD2.

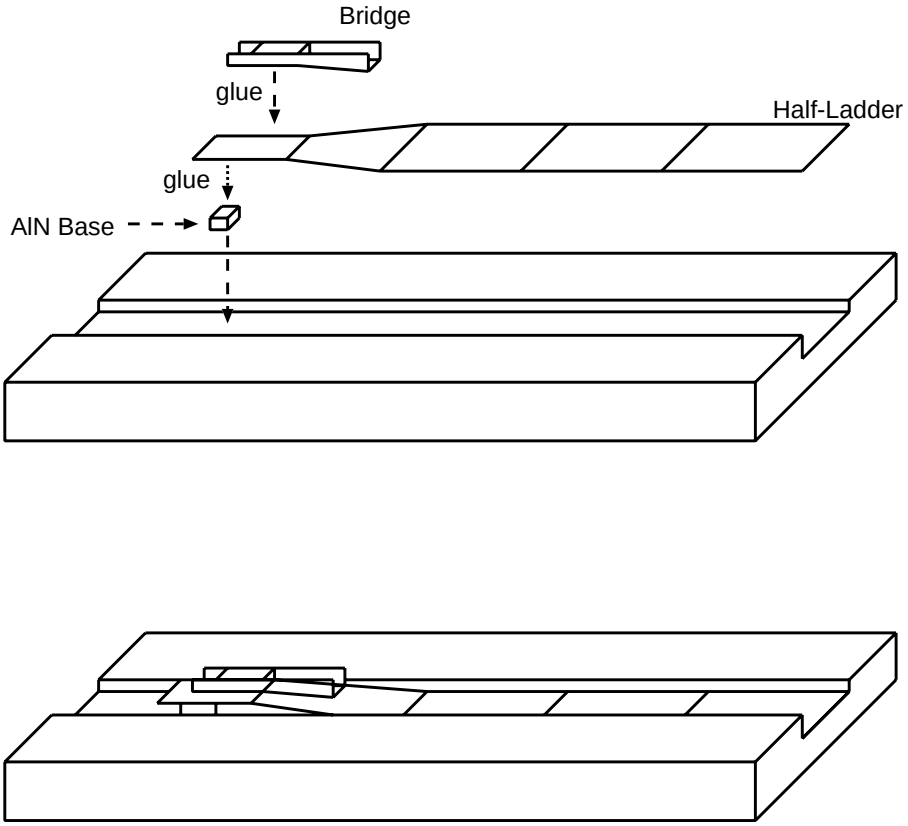


Figure 3.17: Full-ladder assembly 1
Gluing ALN base and bridge to hal-fladder

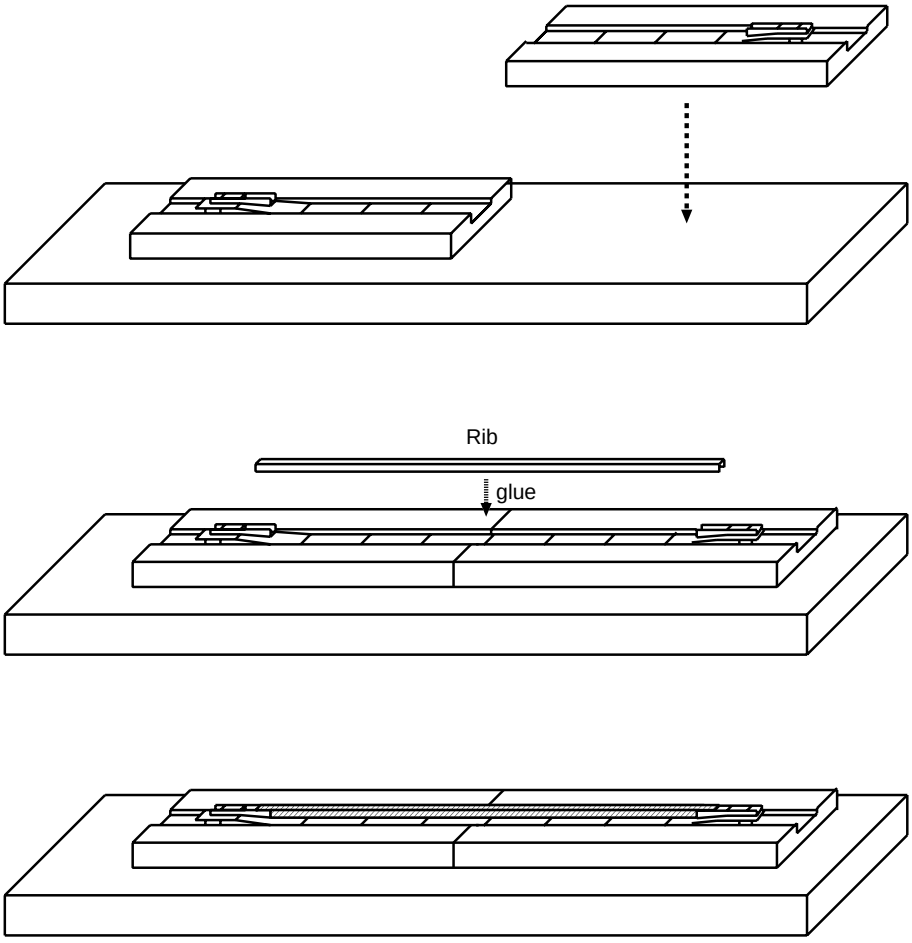


Figure 3.18: Full-ladder assembly 2
Set two half-ladders on the base fixture and gluing rib

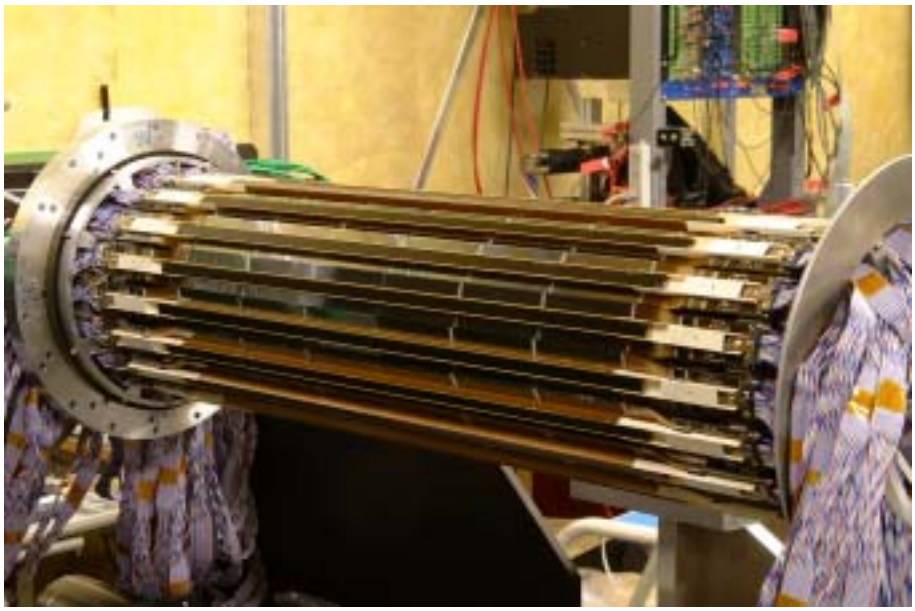


Figure 3.19: SVD2 (ladder mount completed)

3.6 Readout test

Readout test is done in each assembly stage: receiving hybrids, after gluing, after wire-bonding, after full-ladder assembly, after delivering to KEK, and before and after ladder mounting. We use "VA-DAQ" (see Fig.3.20), which is provided by IDEAS, to operate the VA1TA chip. The VA-DAQ provides the detector bias voltage and current, the clock, the hold signal, the serial shift register mask, and the test pulse.

The VA-DAQ can read out both the analog and trigger outputs channel-by-channel. The VA-DAQ is controlled with a PC (the OS must be WINDOWS 95 series) through a parallel port. All analog outputs from the VA1TA chip are digitized on the VA-DAQ and read out by the PC. A drawing of the readout test system is shown in Fig.3.21. It consists of VA-DAQ, PC, power supplies for VA-DAQ system and detector biasing.

Figure 3.20: VA-DAQ

Detector bias value used in the readout test is shown in table 3.4. Because we can't apply the bias voltage on both sides of the DSSD in the test system, we set reading side ground level and the other side ± 80 V. The difference of voltage of p and n sides is the same as case of real system.

When there is no signal, the output of VA1TA contains the offset (pedestal), the intrinsic noise of VA1TA and possible shift common to all strips within a

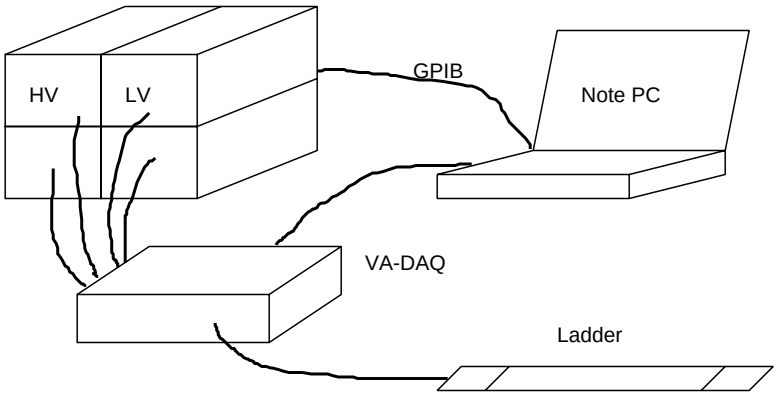


Figure 3.21: Test set up

Table 3.4: Detector bias

	p-side	n-side
VA-DAQ (readout p-side)	-80 V	0 V
VA-DAQ (readout n-side)	0 V	+80 V
Real System	-40 V	+40 V

chip (common mode shift). The source of common mode shift is fluctuation of bias voltage and external electric noise in the readout path. We measure the pedestal and noise of each channel by taking data without any external input. The pedestal of i-th channel (ped^i) is calculated using n events as

$$ped^i = \frac{1}{n}\sum_{j=1}^{n} adc_j^i, \tag{3.1}$$

where adc_j^i is the value of ADC count of i-th channel in j-th event. The common mode shift in j-th event (cms_j)is calculated as

$$cms_j = \frac{1}{N}\sum_{i=1}^{N}(adc_j^i - ped^i), \tag{3.2}$$

where N is the number of the strips in a VA1TA chip (=128). We define the noise of each strip (σ^i) as the rms of the output after subtracting pedestal and common mode shift:

$$\sigma^i = \sqrt{\sum_{j=1}^{n}(out_j^i - < out^i >)^2}, \tag{3.3}$$

$$out_j^i = adc_j^i - ped^i - cms_j, \tag{3.4}$$

$$< out^i >= \frac{1}{n}\sum_{k=1}^{n} out_k^i. \tag{3.5}$$

The test pulse is converted from voltage to charge in capacitors mounted on hybrids. Test charge of -5 $\sim$ +5 fC ($\pm$ 1.6 MIP equivalent) are injected and the output values of VA1TA are measured as a function of input charge. We calculate the gain of each channel from the slope of the output vs. input.

Pedestal, noise, gain, and TA threshold of every channel is measured in each step during the ladder assembly to find any problem. Typical result is shown in Fig.3.22.

3.7 Ladder Mechanical Test

We performed several mechanical test to confirm the deformation of ladder during operation is small enough. Here we present the results o the tests.

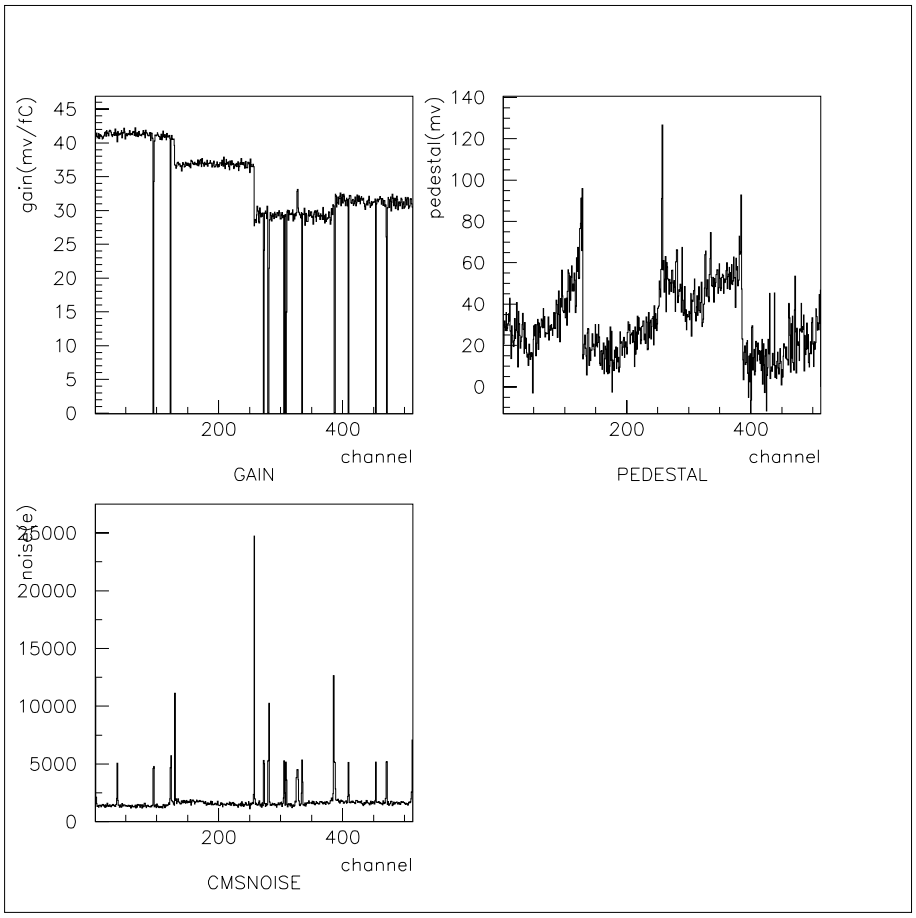


Figure 3.22: Typical result of the readout test using VA-DAQ
The measured gain (top left), pedestal (top right), and intrinsic noise (bottom) of each channel are shown for a hybrid

3.7.1 Sliding Mechanism

SVD2 is constructed in room temperature ($\sim$ 25°C). On the other hand, the operation temperature of the ladder is $\sim$ 15°C. In order to prevent the ladder from breaking because of its thermal expansion (or contraction), the ladder has sliding mechanism. This mechanism consists of an oval-shaped hole and a pin. Fig.3.23 is a conceptual diagram and a picture of sliding mechanism. This mechanism allows a ladder to slide in z direction without r-ϕ motion, and thermal expansion (or contraction) is absorbed by this 500 μm-gap.

We test this mechanism using a dummy ladder made from real material. The dummy is set on an aluminum table (see Fig.3.24). Backward side is rigidly fixed on the base with a screw. On the other hand, forward side is loosely fixed. All system is heated and cooled in thermostatic oven. The forward side screw is tighten by torque 0, 0.5, and 1.0 kgf·m. Fig.3.25 shows the result. Horizontal axes represents the temperature and vertical axes represents the difference of length between the ladder and the Al table. Open circles results during heating, while solid triangles are during cooling.

The ladder is sliding in the cases of (a) and (b), but tensioned in the case of (c). In order to assure the ladder sliding, we need to set the torque value for the tighten screw less than about 0.5 kgf·m. This test is done under very extreme condition: the difference of the thermal expansion coefficient between the ladder and the Al table is very large. On the other hand, in real operation, the ladder and the support structure (the end ring) are expected to have close thermal expansion coefficient (see Table.3.1). We conclude that the sliding mechanism works properly if we tighten the forward side screw by 0.5 kgf·m.

3.7.2 The Sag of the Ladder by Tension and Weight

We check the amount of the the sag of the ladder when the ladder is compressed longitudinally. Fig.3.26 shows the sag of the center of the ladder when we push the ladder from one side, while another side is fixed. Horizontal axis represents the length that we push the ladder, and vertical axis means sag of the center of the ladder. As described in Sec.3.7.1, temperature change of the ladder is $\sim$ 10°C in the maximum. It corresponds to 25 μm difference of length between the ladder and the support structure (the end ring). If the ladder doesn't slide at all, the sag is 14 μm from Fig.3.26. This value is small enough.

Fig.3.27 shows the sag of the center of the ladder when we set the weight on the center of the ladder. From this plot, sag by weight is 1.2 μm/g. On the other hand, from FEA simulation, sag by weight is 1.7 μm/g. Test result is consistent with the simulated value. This proves that our design concept is proper and the ladder has desired strength.

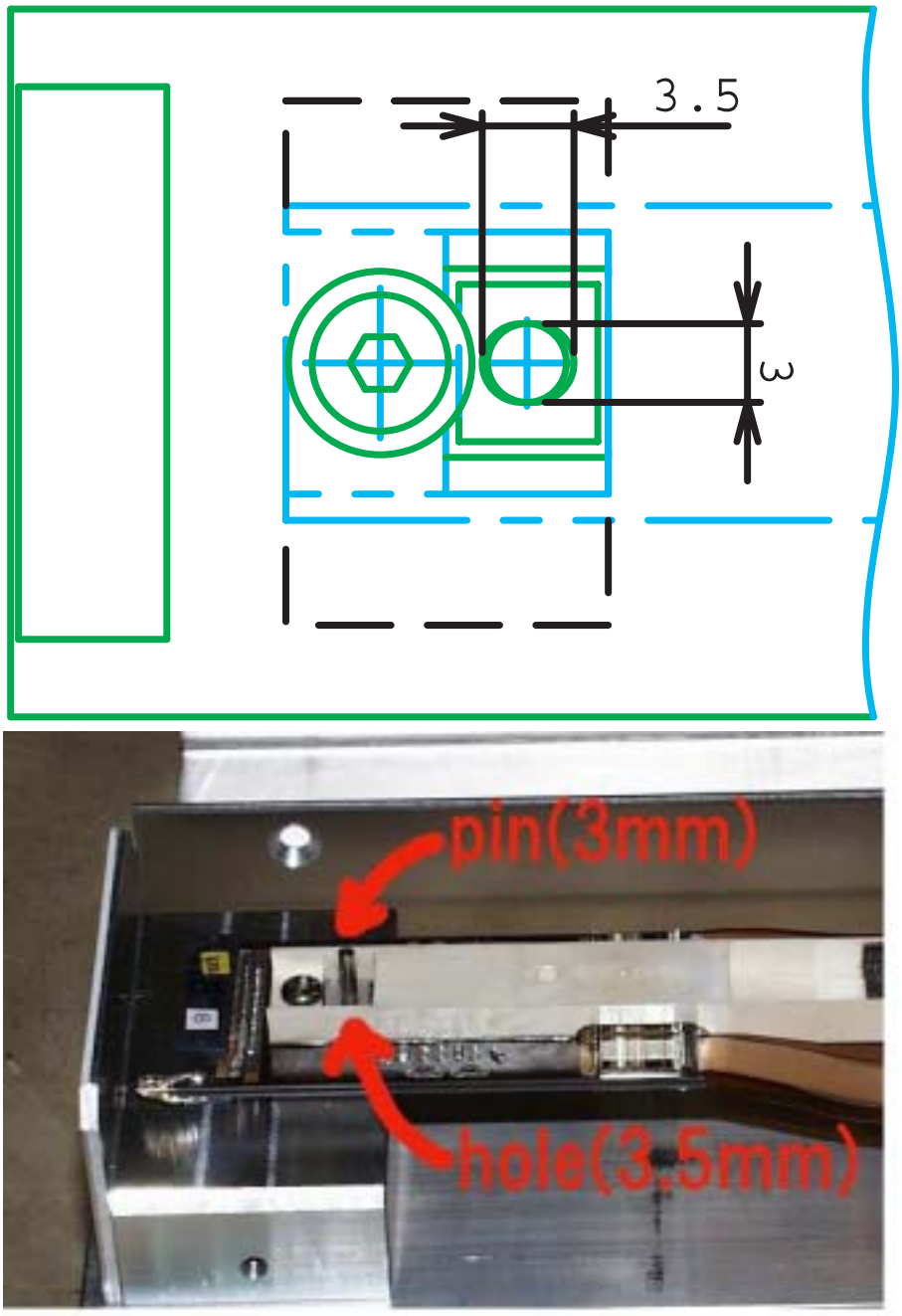


Figure 3.23: A conceptual diagram and a picture of sliding mechanism

Figure 3.24: Test set up for sliding mechanism
A dummy ladder is set on the aluminum base.

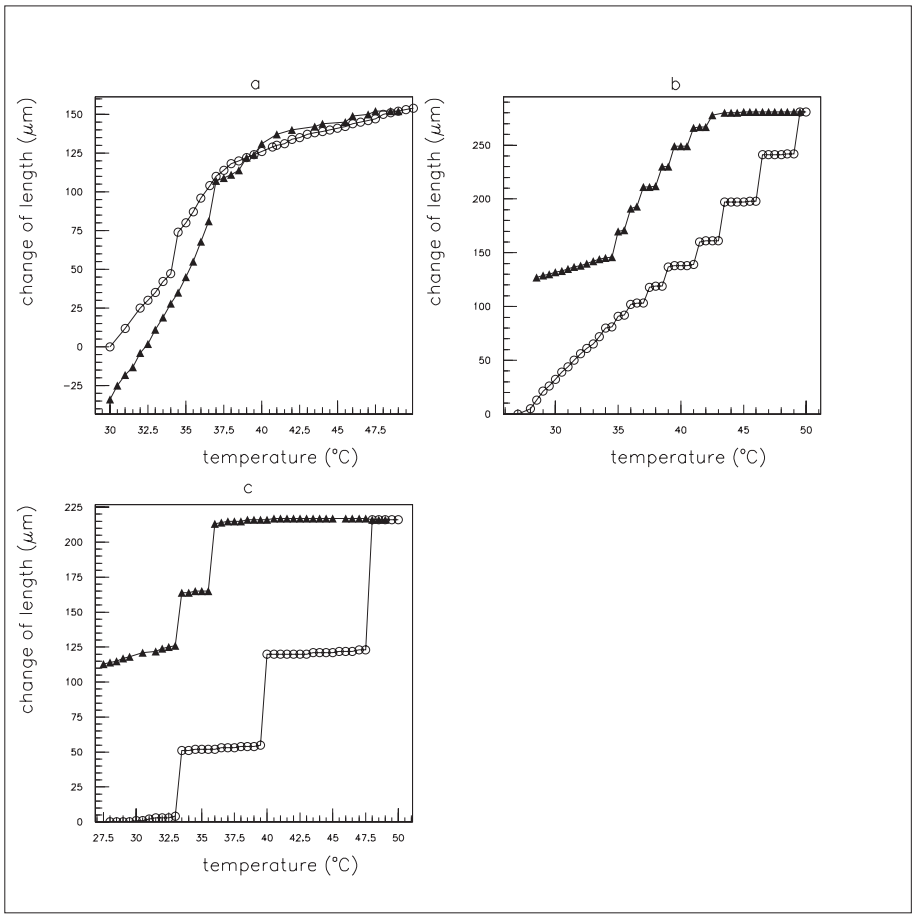


Figure 3.25: Result of sliding mechanism test
∘ means results during heating, △ are during cooling. We tighten the forward side screw by 0 (a), 0.5 (b), 1.0 (c) kgf·m

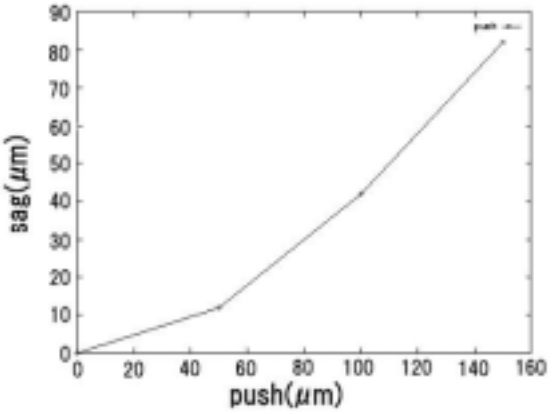


Figure 3.26: The sag of the center of the ladder when we push the ladder from one side

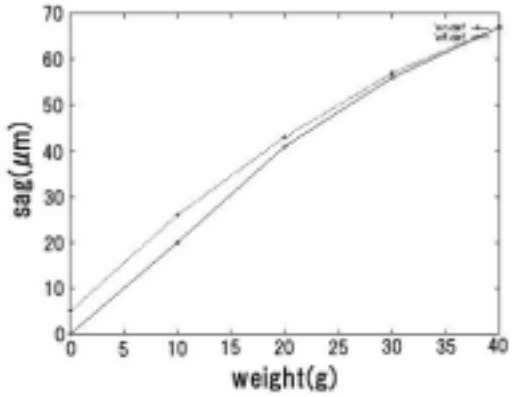


Figure 3.27: The sag of the center of the ladder when we set the weight on the center of the ladder

Chapter 4

Performance

In this chapter, we describe the performance of SVD2. After describing basic performance, we present preliminary results of the cosmic ray test.

4.1 Basic Performance

4.1.1 Strip Yields

Strip yields of each layer are shown in table.4.1, 4.2, 4.3, and 4.4. We define the bad channel as the channel with the noise which deviate more than three times of the root mean squares of noise distribution from the mean value of a VA1TA chip or the channel that flex circuit is breaking. Main sources of a bad channel are DSSD bad strip (AC-coupling break-down), short of bonding wire, and short of flex circuit. All the hybrids have strip yield better than 94%. Average yields of each layer is better than 96%. This is satisfactory for the vertex measurement.

Table 4.1: Strip yields for layer-1

Ladder#	Forward(p)	Forward(n)	Backward(p)	Backward(n)
0	0.971	0.976	0.975	0.974
1	0.976	0.960	0.973	0.979
2	0.990	0.968	0.978	0.964
3	0.984	0.981	0.984	0.964
4	0.982	0.976	0.978	0.968
5	0.961	0.966	0.975	0.972
Average	0.974			

Table 4.2: Strip yields for layer-2

Ladder#	Forward(p)	Forward(n)	Backward(p)	Backward(n)
6	0.967	0.966	0.970	0.966
9	0.965	0.972	0.954	0.970
10	0.976	0.985	0.954	0.978
11	0.967	0.985	0.950	0.976
12	0.971	0.974	0.950	0.978
13	0.967	0.972	0.954	0.974
14	0.969	0.968	0.950	0.976
15	0.980	0.964	0.956	0.974
16	0.975	0.978	0.960	0.968
17	0.959	0.966	0.942	0.978
Average	0.968			

Table 4.3: Strip yields for layer-3

Ladder#	Forward(p)	Forward(n)	Backward(p)	Backward(n)
22	0.944	0.964	0.950	0.962
23	0.958	0.974	0.953	0.987
24	0.960	0.976	0.963	0.976
25	0.962	0.980	0.953	0.970
26	0.946	0.974	0.953	0.978
27	0.950	0.964	0.965	0.958
28	0.954	0.978	0.963	0.981
29	0.966	0.972	0.969	0.978
30	0.964	0.976	0.949	0.970
31	0.966	0.974	0.938	0.983
32	0.944	0.978	0.951	0.976
33	0.964	0.980	0.961	0.978
Average	0.967			

Table 4.4: Strip yields for layer-4

Ladder#	Forward(p)	Forward(n)	Backward(p)	Backward(n)
40	0.954	0.977	0.958	0.971
41	0.966	0.983	0.968	0.977
42	0.968	0.983	0.962	0.983
43	0.960	0.979	0.962	0.981
44	0.954	0.979	0.968	0.981
45	0.960	0.979	0.960	0.979
46	0.966	0.985	0.956	0.979
47	0.960	0.981	0.958	0.981
48	0.958	0.981	0.962	0.981
49	0.964	0.977	0.962	0.981
50	0.954	0.981	0.962	0.979
51	0.964	0.981	0.962	0.983
Average	0.970			

4.1.2 Noise and Gain Measurement

Noise and gain are measured with the same procedure as VA-DAQ test (Sec.3.6).

Figs.4.1 and 4.2 show the distribution of average noise of VA1TA chip for each type of half-ladders. Noise level depends on the number of DSSD which is connected to the hybrid. The number of DSSD connected to the hybrid is shown in table.2.2. Since layer-4 ladders have different type of DSSD from layer-1–3, we treat layer-4 separately. Fig.4.3 shows the average gain of each VA1TA. These values are consistent with VA-DAQ measurement during detector assembly.

4.2 Cosmic Ray Test

In the previous section, we have confirmed that the basic performance of SVD2 is satisfactory. In this section, we present the result of cosmic ray test to further evaluate the performance.

Because of a delay in the ladder production schedule, we couldn't mount all ladders when we did the performance test (Dec. 2002). Fig.4.4 shows the status of the ladder mounting at that time. The mounted ladders are indicated by solid lines, while broken lines indicate not-mounted ones. Remaining ladders will be mounted by Feb. 2003.

Although some ladders were not mounted, cosmic ray test was done using the real readout system (shown in Sec.2.3.5). We used two scintillation counters as the readout trigger. They were set above and below SVD2 (see Fig.4.4) and coincident signal was used to trigger the readout system.

Figs.4.5 and 4.6 are schematic displays of a real cosmic ray event (r-ϕ view and z-view). Dashed and solid lines indicate the cosmic ray track found by the

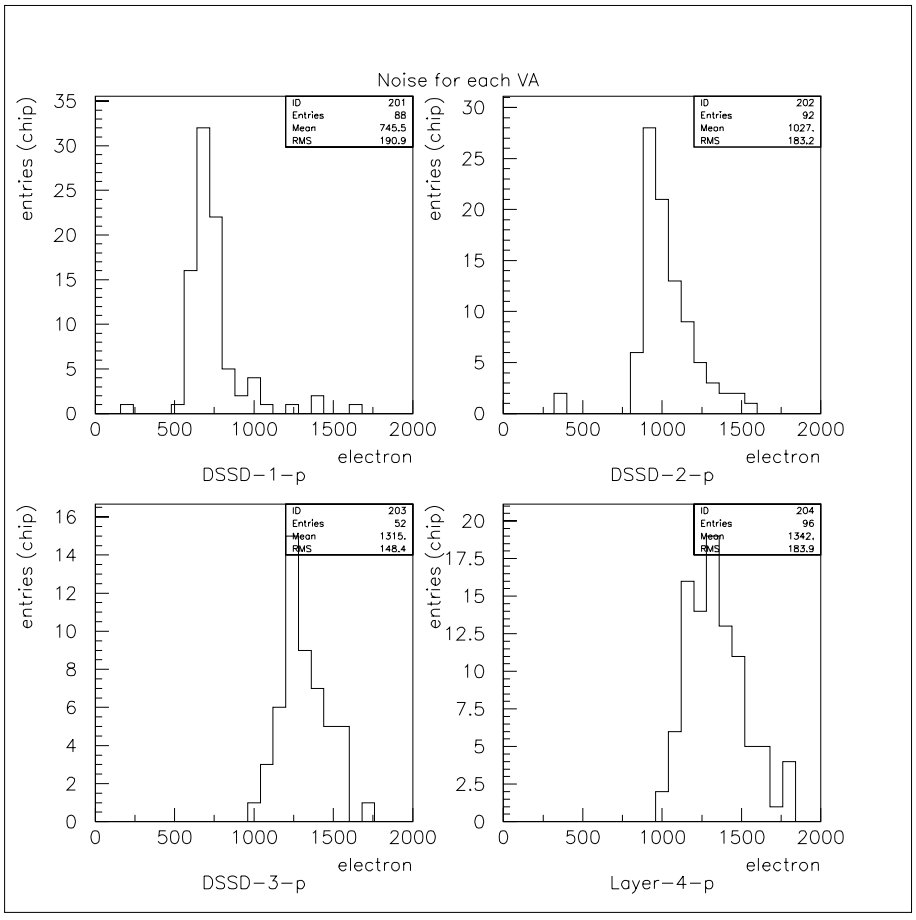


Figure 4.1: Average noise of each VA1TA chip connected to the p-side of DSSD Results are shown in each half-ladder type: one (top-left), two (top-right), three (bottom-left) DSSD in layer 1–3, and layer-4 (bottom-right).

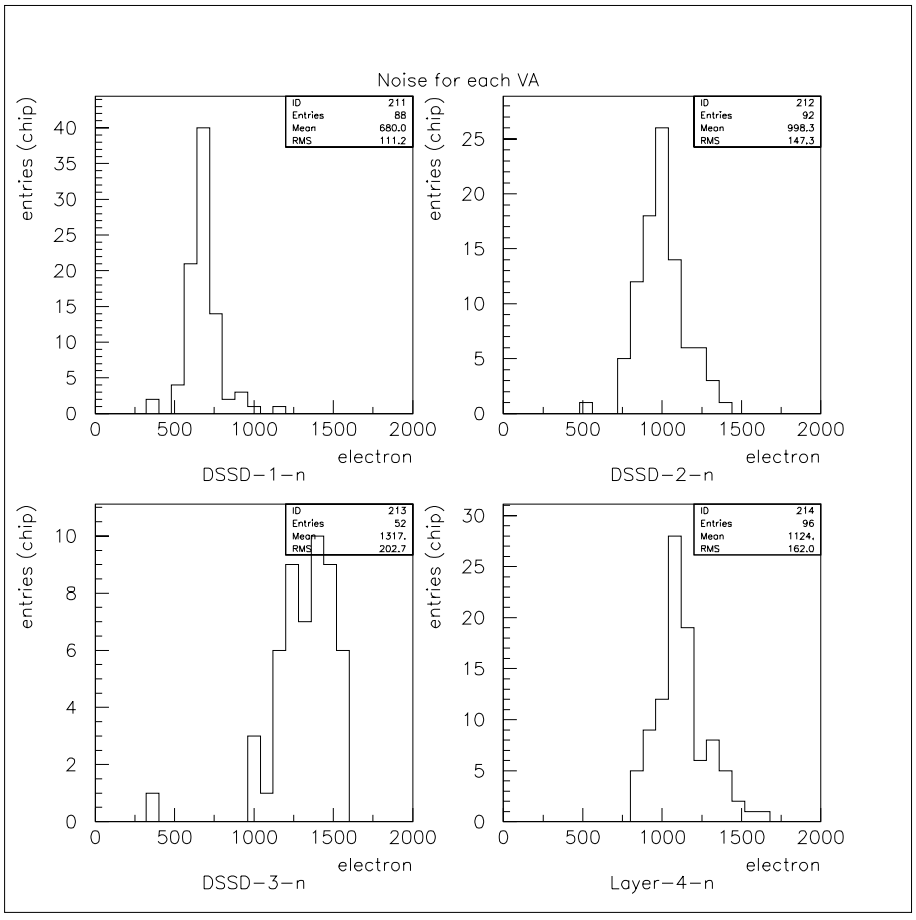


Figure 4.2: Average noise of each VA1TA chip connected to the n-side of DSSD Results are shown in each half-ladder type: one (top-left), two (top-right), three (bottom-left) DSSD in layer 1–3, and layer-4 (bottom-right).

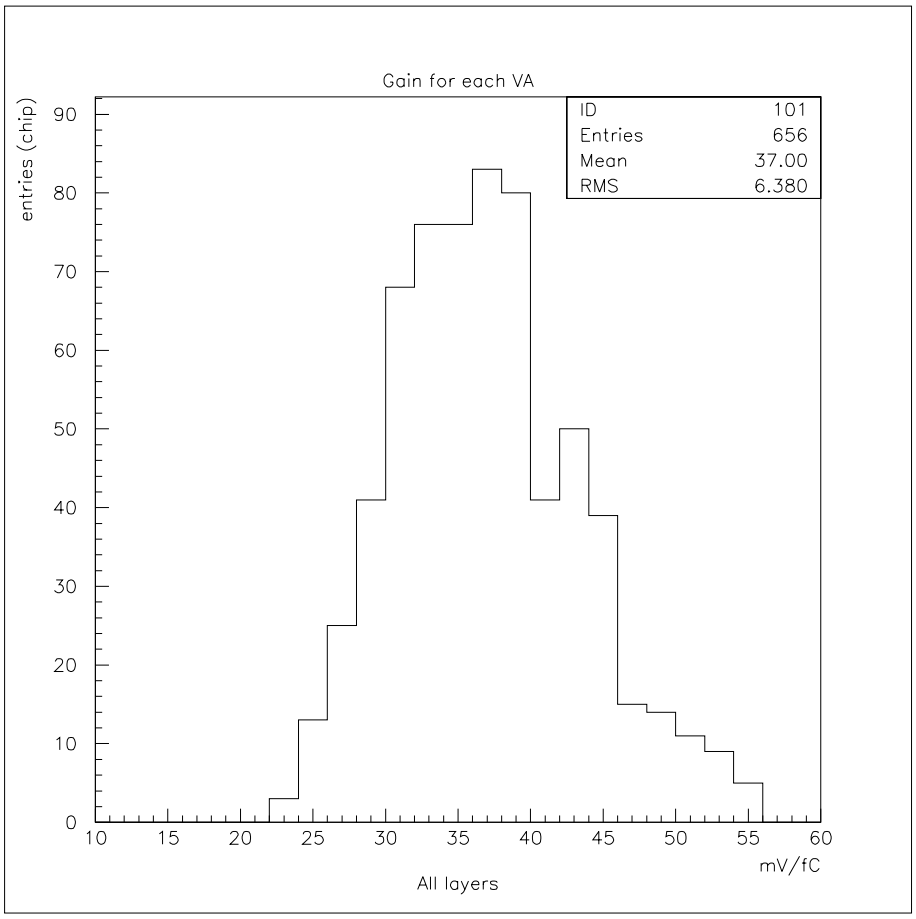


Figure 4.3: Average gain of VA1TA chip

Figure 4.4: Configuration of cosmic ray test (solid lines indicate mounted ladders, and broken lines indicate unmounted ladders)

SVD self-tracking software. Track fitting is done by the least squares method. We require more than six 2-D hits for a cosmic track.

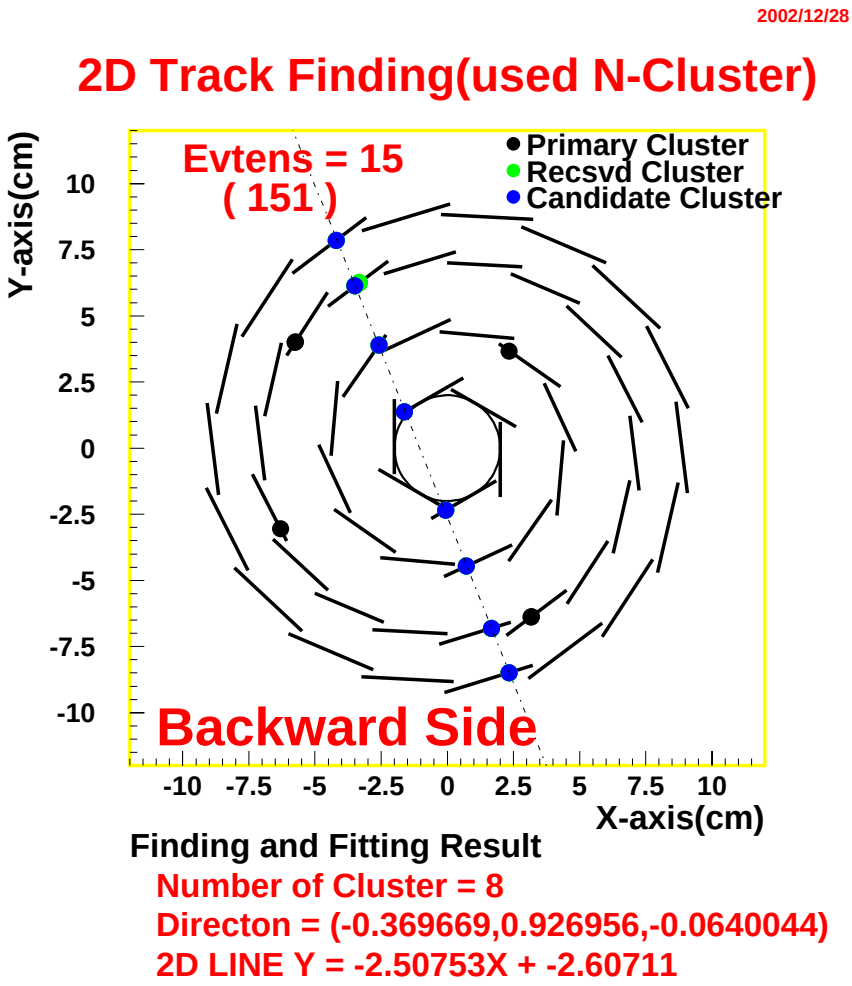


Figure 4.5: A cosmic ray event reconstructed by SVD2 (r-ϕ-side)

4.2.1 Pulse Height Distribution

Figs.4.7 and 4.8 show the pulse height distributions (in the unit of electron) of cosmic ray events for p and n channels, respectively. We choose the hits which are used to reconstruct the tracks. The small peaks below 5000 e^- are due to noise hits.

Fitting with Landau distribution, we estimate the most probable pulse height: 19140 $\pm 38 e^-$ for p-side, 19200 $\pm 32 e^-$ for n-side.

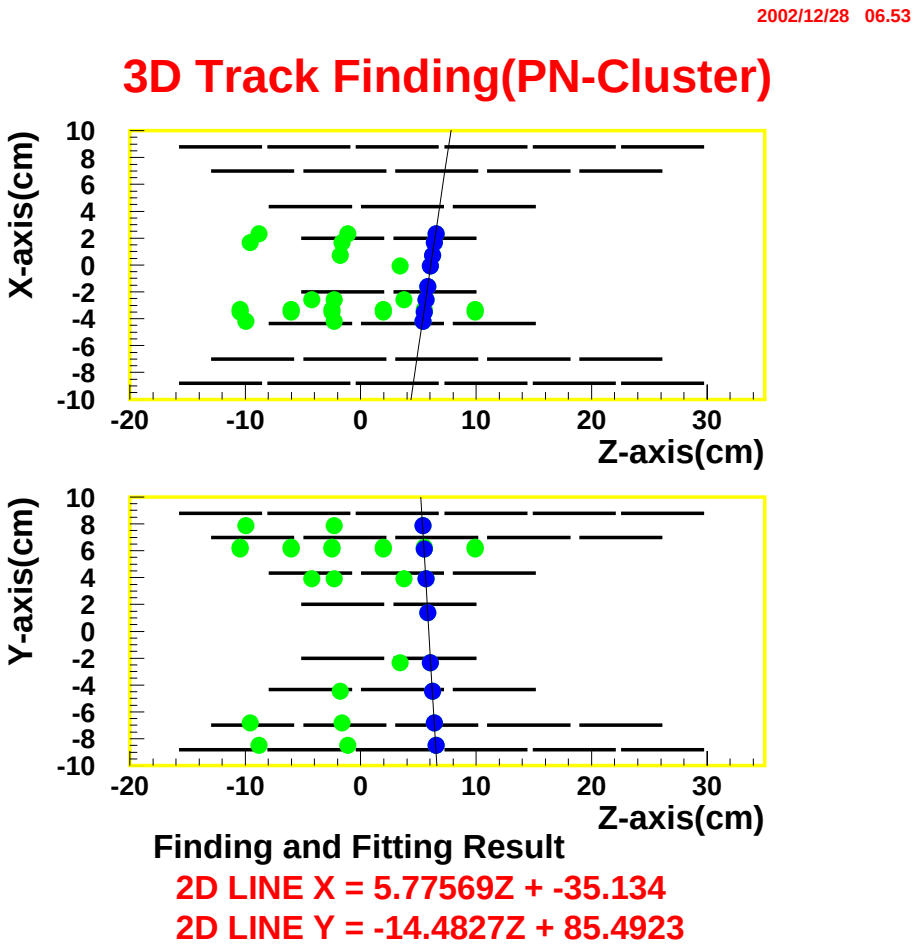


Figure 4.6: A cosmic ray event reconstructed by SVD2 (z-side)

The energy loss of minimum ionizing particle (MIP) in 300 μm Si is about 80 keV. On the other hand, the energy which is needed to create an electron-hole pair is 3.6 eV in Si. Therefore, about 22000 electron-hole pairs are created in DSSD. Assuming the efficiency to detect electron-hole pairs is 90 %, we will obtain about 20000 e^- by the MIP. Since calibration of preamplifier gain and tuning of parameters are still preliminary, we consider the measured pulse height is reasonable. Fig.4.9 shows the pulse height correlation. Horizontal axis represent p-side, vertical axis represent n-side.

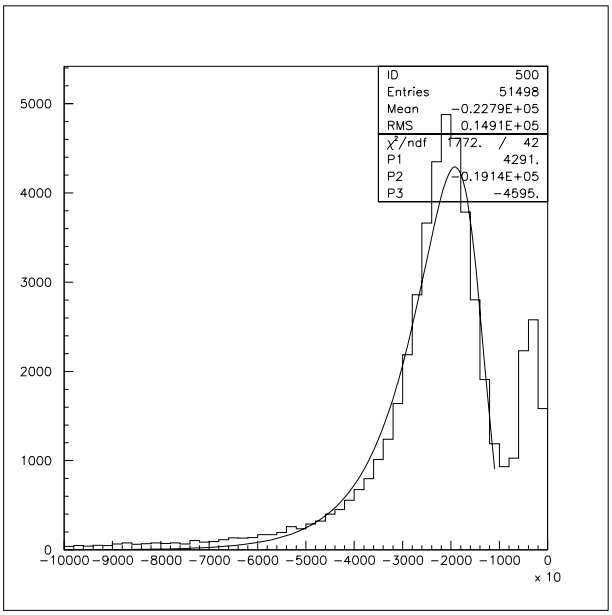


Figure 4.7: Pulse height distribution for p-side

4.2.2 Signal to Noise Ratio

From the pulse height that we present in the previous section, we calculate the signal to noise ratio.

Table.4.5 shows the noise and S/N ratio for each type of half-ladder. The minimum S/N ratio required for proper cluster-finding in our configuration and readout system is about 10 from our experience using SVD1. Therefore, we conclude that the measured S/N is good enough for all layer.

4.2.3 Hit Efficiency

Table.4.6 shows the hit efficiency of each layer. We define the hit efficiency as the number of found hit points divided by the number of expected hit points

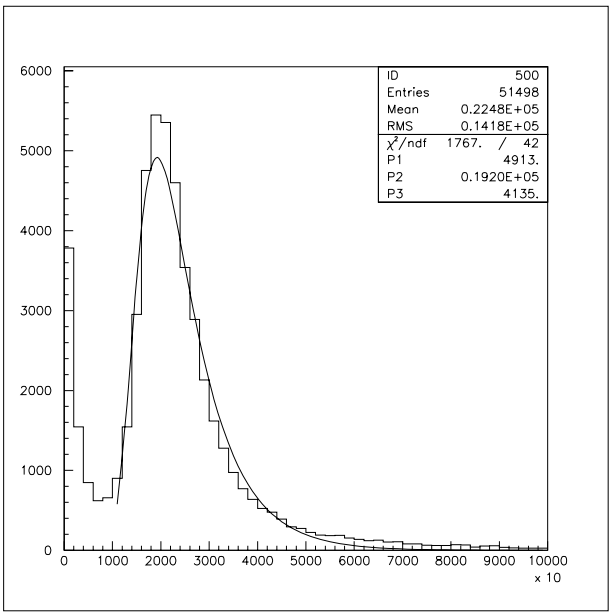


Figure 4.8: Pulse height distribution for n-side

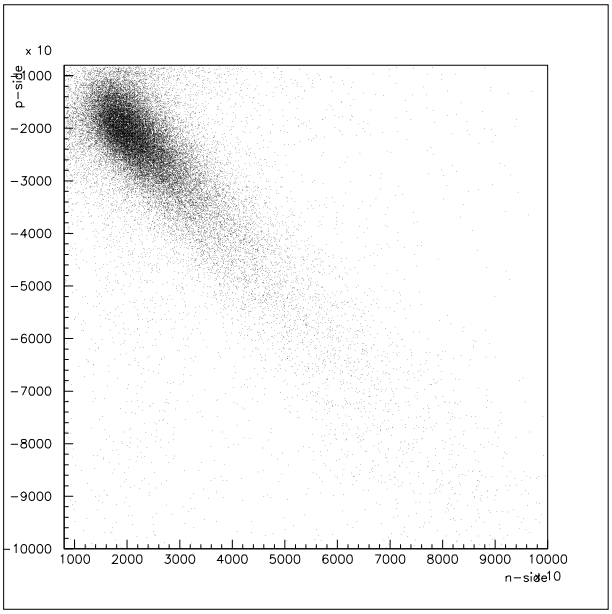


Figure 4.9: Pulse height correlation (p-side and n-side)

Table 4.5: Signal to noise ratio

	p-side				n-side			
Type of DSSD	Layer-1∼3			Layer-4	Layer-1∼3			Layer-4
The number of DSSD	1	2	3	3	1	2	3	3
Noise (electron)	746	1027	1315	1342	680	998	1317	1124
S/N	25.7	18.6	14.6	14.3	28.2	19.2	14.6	17.1

Table 4.6: Hit efficiency

Layer	1	2	3	4
Efficiency (%)	94.9±0.6	97.5±0.4	92.3±0.7	95.1±0.6

from fitted tracks.

Efficiency of all layers are better than 94% except layer-3. We suspected that strip yield of layer-3 is worse than others. But as shown in Sec.4.1.1, there is no significant difference of strip yield between layer-3 and others. Fig.4.10 shows the position distribution of hits used to reconstruct tracks. We do not see inefficient region in layer 3. We need more detailed study to understand the reason.

4.2.4 Residual Distribution

Figs.4.11 and 4.12 show residual distributions of a DSSD in z- and r-ϕ-direction. Z-axis is defined in Figs.4.5 and 4.6. Residual is defined as the distance between the measured hit point and the point where fitted track crosses the DSSD plane.

The residual distributions are fitted using double-Gaussian. Broad Gaussian is considered to be the tail caused by miss alignment and noise hit. Therefore, we take the narrow Gaussian to represent the detector resolution. σ of narrow Gaussians of Figs.4.11 and 4.12 are 36.3±2.1 μm and 103±5.8 μm, respectively.

The residual is a measure of the detector resolution. However, its dispersion includes not only the intrinsic resolution of the DSSD, but also the alignment precision and the error of fitted tracks.

In the current analysis, the alignment of the detector position has not been performed. Therefore, the values quoted above do not represent the ultimate performance, but they indicate the resolution of the detector is reasonable.

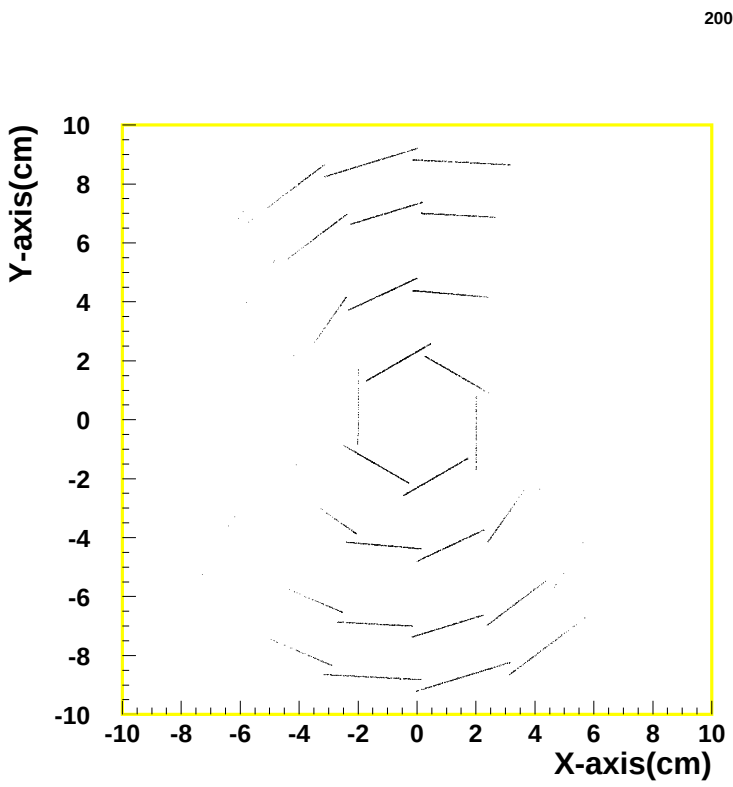


Figure 4.10: Position distribution of hits used to reconstruct cosmic tracks

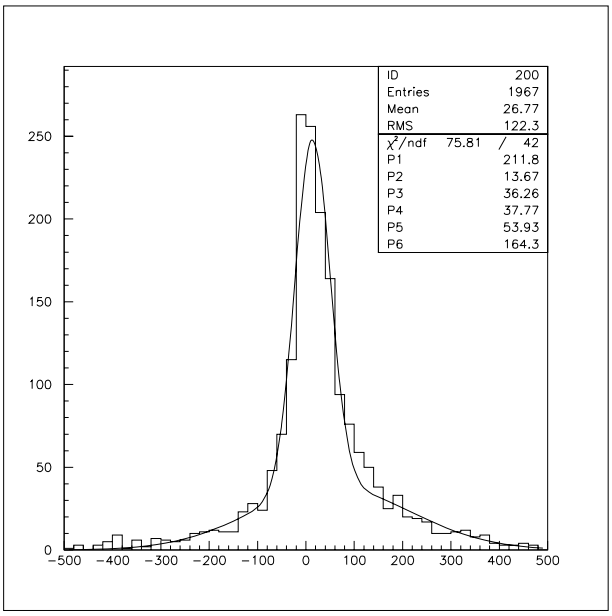


Figure 4.11: Residual distribution (z-axis)

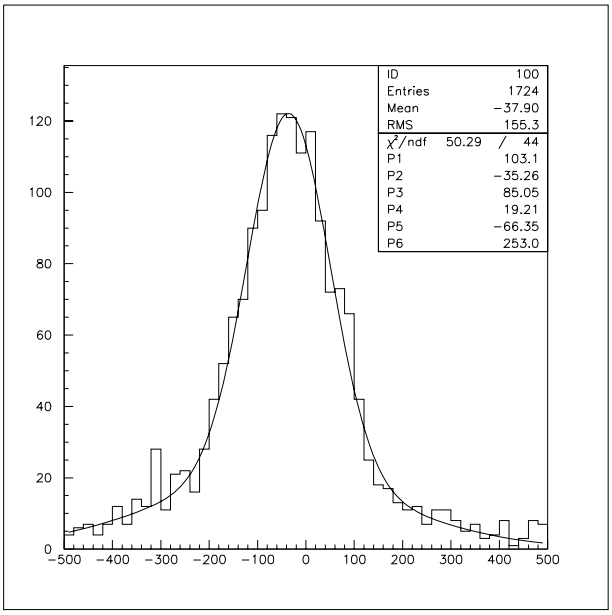


Figure 4.12: Residual distribution (x-axis)

Chapter 5

Conclusion

The Silicon Vertex Detector (SVD) is the most important component of the Belle detector for time-dependent analyses in the KEK B-Factory experiment. Based on the successful experience with the current SVD (SVD1), we plan to upgrade the Belle SVD in summer 2003 to improve its performance. Major improvement of the upgraded SVD (SVD2) are : 1) increase of layers from 3 to 4 2) smaller radius of inner-most layer 3) larger angular acceptance and 4) better radiation tolerance.

While the increase of the numbers of layers enables us to achieve better efficiency, the length of the ladder becomes much longer than that of SVD1 in outer layers. In addition, we have newly introduced flex circuit to connect the DSSD and front-end readout chip. Therefore we have developed a new procedure to assemble the ladder of SVD and successfully assembled all the necessary ladders.

We have tested SVD2 with the real readout system. We have confirmed that the strip yield is better than 96% and S/N ratio is better than 10 for all layers, which satisfy our requirements. Using cosmic rays, we have shown that we are able to detect and reconstruct tracks. Although tuning and calibration of the system are still ongoing and the results are very preliminary, we have confirmed that the SVD2 is properly working.

Due to a delay in the assembly schedule, some of the ladders have not been mounted onto the detector structure. The remaining ladders will be mounted by Feb. 2003. After further test and tuning, SVD2 will be installed into the Belle detector in summer 2003.

Appendix A

Principle of Silicon Strip Detector

The semiconductor detectors, originally used for the energy measurement of an ionizing particle in nuclear physics, are now widely used in particle physics experiments. In particular, their capabilities of a precise position measurement make the silicon detectors very popular device in particle physics experiment in which accurate position measurement is required.

In this chapter, the fundamentals of the semiconductor devices and the principle of the silicon strip detector are described.

A.1 Semiconductor Device

In a perfect crystal, electron energies are constrained to lie in bands. The valence band and conduction band are separated by an energy gap in which no electrons are allowed. The electrons in valence band are excited thermally to conduction band. The electrons missing in the valence band are called holes. For an intrinsic semiconductor, the number of electrons is equal to the number of holes.

The semiconductors are usually doped with small fraction of impurities to produce additional states in the originally forbidden energy gap. The impurity atoms with one additional electron in the outer shell (e.g. phosphorus or arsenic) are called "donor" and those with one less valence electron (e.g. boron in silicon) called "acceptor". In the n-type (doped with donor atoms) semiconductors, almost all electrons from donor states situated close to conduction band move into the conduction band because of the high density of available free states in the band. This causes a shift of the Fermi level from the gap center toward the conduction band and a decrease in the density of the holes in the valence band. In the p-type (doped with acceptor atoms) materials, an increase of the hole densities and a decrease of the electron densities are caused by similar effects.

A.1.1 p-n junction

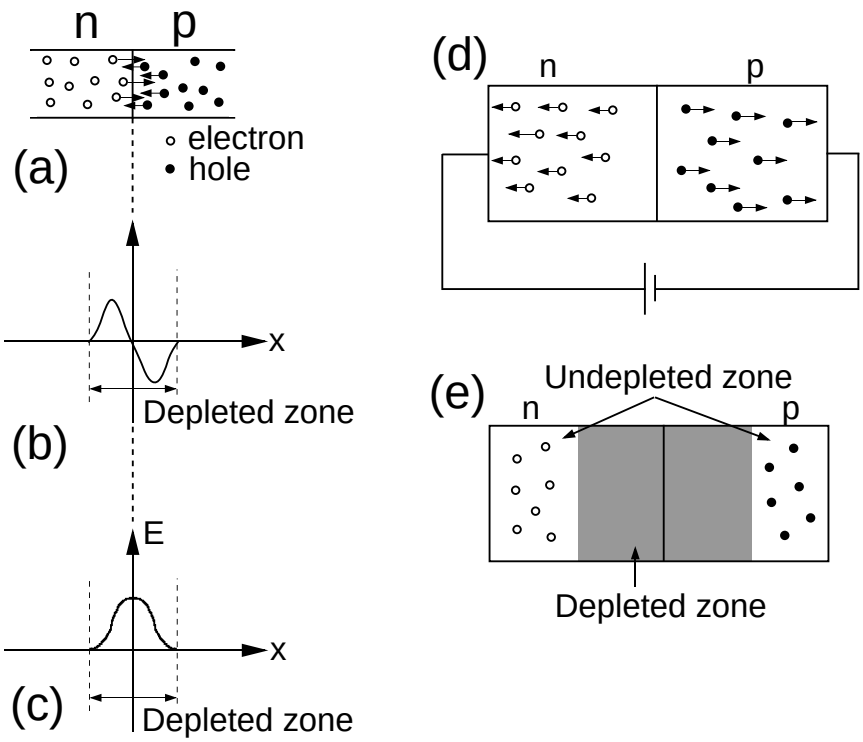


Figure A.1: Schematic drawing of the p-n junction.

The band structures of the p and n semiconductors are shown in Fig. A.1(a). Once they are brought into contact, the electrons and holes drift into the p-region and the n-region, respectively. This causes an excess of the negative charge in the p-region and the positive charge in the n-region. As a result, the electric field is created and any movable charge carriers (electrons and holes) are swept out from the region around the boundary, resulting in a space charge region. Figures A.1(b) and (c) show the carrier density and the electric field distributions, respectively.

If the negative voltage on the n-side and the positive voltage on the p-side are applied, the movable charge carriers are pushed toward the junction, and the electrons and holes recombine near the interface and current flow. When the voltage in the opposite direction is applied, the electrons and holes are pulled away and the space charge region increases as shown in Figs. A.1(d) and (e).

A.2 Silicon Strip Detector

Strip detectors are in principle large area diode divided into the narrow strips, each of which is read out by a separate electronic circuit. The detector consists of a highly doped p^+ region on a low doped n^- substrate, the backside of a highly doped n^+ layer. Usually, a reversed bias is applied to fully deplete the substrate, making the sensitive area wider and the number of produced charge greater.

The charged particles passing through the detector ionize atoms in the depletion region to produce electron-hole pairs. The generated electrons and holes are separated by the strong electric field and the electrons (holes) drift towards n^+ (p^+) electrode. The position of the charged particle is given by the location of the strip carrying the signal. The signal from the detector is read out as amount of the charge collected in the electrode. It is converted into the voltage by a charge amplifier and sent to the ADC.

The nominal thickness of a silicon strip detector is 300 μm and the required energy to produce an electron-hole pair is 3.6 eV in the silicon. A minimum ionizing particle deposits about 80 keV of its energy into a 300 μm thick silicon detector and creates about 22000 electron-hole pairs.

The single-sided strip detectors described above make use of only one type of the charge carrier, usually holes. By dividing the backside n^+ layer into the strips and using the electrons collected there, a second coordinate can be read out from the same wafer (Fig A.2). This is the principle of the double-sided silicon strip detector (DSSD). Since two-dimensional information can be obtained by one silicon wafer, we can reduce the effects of the multiple scattering by using the DSSD.

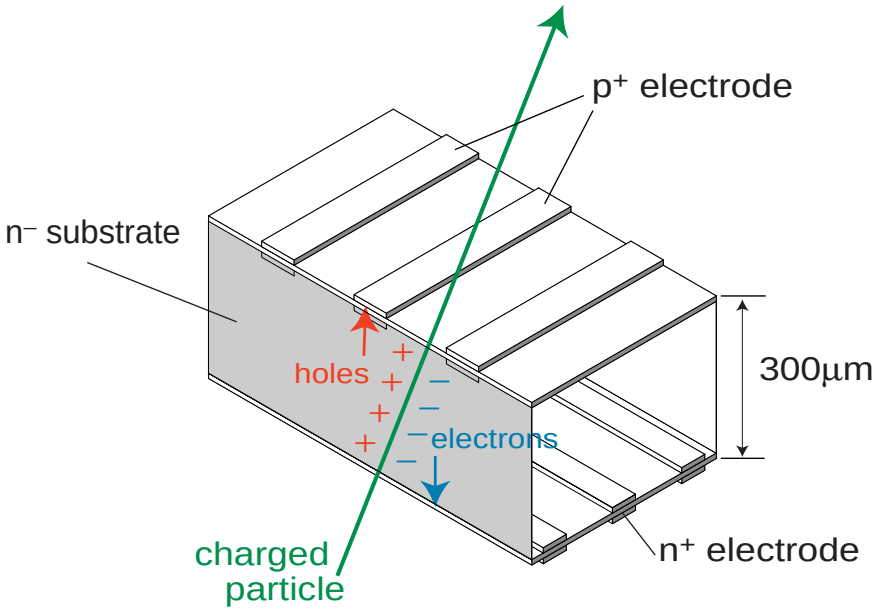


Figure A.2: Schematic drawing of the Double-sided Silicon Strip Detector (DSSD).

Acknowledgement

At first I would like to express my thanks to my supervisor H.Aihara. I am thanksfull to M.Iwasaki for her advice.

I would like to express my appreciations to J. Haba, M. Hazumi, Y. Yamada, T. Tsuboyama, Y. Ushiroda, T. Kawasaki, H. Ishino, Y. Igarashi, T. Higuchi and all the member of Belle SVD group.

I thanks to students of SVD group, T. Mori (TIT), F. Ohno (TIT), Y. Onuki (Niigata-U), T. Shibata (Niigata-U), Y. Harada (Niigata-U), H. Matsumoto (Niigata-U), M. Watanabe (Niigata-U), H. Terazaki (Tsukuba-U), Y. Nakano (Tsukuba-U) for fruitful discussions and joyful drinking.

N. Sato, R. Okubo, and S. Koike (KEK machine shop). H. Mori, M.Honda, R. Kyushima and K. Fujita (HPK).

I also thank all the members in our lab, M. Yokoyama, T. Tomura, T. Nakadaira, H. Kawai, Y. Yamashita, A. Kusaka, K. Tanabe, and R. Ishida.

Bibliography

[1] T. D. Lee and C. N. Yang, Phys. Rev. Lett. **98** 1501 (1955); Phys. Rev. Lett. **104** 254 (1956).

[2] C. S. Wu *et al.*, Phys. Rev. Lett. **105** 1413 (1957).

[3] J. H. Christenson, Cronin, Fitch and Turlay, Phys. Rev. **13** 138 (1964).

[4] M. Kobayashi and T. Maskawa, *Prog. Theor. Phys.* **49** 652 (1973).

[5] D.E. Groom *et al.* (Particle Data Group), Eur. Phys. J. **C15** 1 (2000). Eur. Phys. J. **C15**, 1 (2000).

[6] L. Wolfenstein, Phys. Rev. Lett. **51** 1945 (1983).

[7] N. Cabibbo, Phys. Rev. Lett. **10** 531 (1963).

[8] KEK Report No. 2001-157, edited by E. Kikutani, 2001 [Nucl. Instrum. Methods Phys. Res. A.to be published)]

[9] Belle Collaboration, Technical Design Report, KEK Report 95-7 (1995); Belle Collaboration, BELLE Progress Report, KEK Report 96-1; Belle Collaboration, BELLE Progress Report, KEK Report 97-1.

[10] A. Abashian *et al.*, Nucl. Instr. Meth. **A479** 117 (2002).

[11] Belle SVD group, Belle SVD Technical Design Report; G. Alimonti *et al.*, Nucl. Instr. Meth. **A453** 71 (2000); R. Abe *et al.*, IEEE Trans. Nucl. Sci. **48** 997 (2001).

[12] E. Nygård *et al.*, Nucl. Instr. Meth. **A301** 506 (1991); O. Toker *et al.*, Nucl. Instr. Meth. **A340** 572 (1994).

[13] M. Yokoyama and H. Tajima, Belle note 196, unpublished.

[14] M. Tanaka *et al.*, Nucl. Instr. Meth. **A432** 422 (1999).

[15] M. Yokoyama *et al.*, IEEE Trans. Nucl. Sci. **48** 440 (2001).