Research and development of magnetized muon range detector and readout electronics for a neutrino cross section experiment

ニュートリノ反応断面積測定実験のための ミューオンレンジ検出器および読み出しエレクトロニクスの 研究開発

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Abstract

For precise measurement of neutrino oscillation, understanding of neutrino interactions on nucleus is indispensable. One of the main systematic errors in neutrino oscillation analysis in the T2K experiment is due to the difference in the acceptance and target materials between Super-Kamiokande and the near detector. In order to reduce this uncertainty, a new experiment, named WAGASCI, at the neutrino beamline in Japan Proton Accelerator Research Complex (J-PARC) has been proposed. Its goal is to measure the cross section ratio of charged current neutrino interaction on nucleus between water target and plastic target with a few percent uncertainty. In this thesis, three topics related to the development of WAGASCI detector are presented.

In order to measure anti-neutrino cross section with the WAGASCI detector, the wrong sign contamination from neutrino in interactions must be reduced. For that purpose, an option to magnetize the downstream muon range detector is proposed. Its performance is evaluated with Monte Carlo simulation.

In the WAGASCI detector, 7760 multi-pixel photon counters (MPPC), produced by Hamamatsu Photonics, will be used. The mass test of MPPCs will use a NIM module with EASIROC, which is a 32-channel fully analog front-end ASIC produced by Omega, as readout electronics. However, the firmware controlling the chips needs to be developed to implement some functions required in the mass test. The new firmware is developed, and its performance is tested.

To read out the MPPCs in the WAGASCI detector in accordance with the J-PARC neutrino beam, new readout electronics with SPIROC are under development. SPIROC is a 36-channel auto-triggered front-end ASIC, and is also produced by Omega. First prototype of the new electronics is produced and its first operation is performed.

Contents

Chapter 1

Introduction

1.1 Physics motivation

1.1.1 Neutrino oscillation

The Standard Model (SM) of elementary particle physics has succeeded in explaining a wide variety of experimental results. However, it is also known that there are phenomena unexplainable by SM, such as the origin of the universe and dark matters. Neutrino oscillation is one of phenomena beyond SM, and an asymmetry between particles and anti-particles (CP violation) in leptons might be observable through it. The lepton CP asymmetry might be a key of the matter-antimatter asymmetry of the universe.

Neutrino is one of leptons in SM, and has three different flavors, electron-neutrino (ν_e), muon-neutrino (ν_μ), and tau-neutrino (ν_τ), and anti-particles for each flavor, $\bar{\nu}_e$, $\bar{\nu}_\mu$, and $\bar{\nu}_\tau$. The SM theory assumes that masses of neutrinos are exactly zero and lepton flavors are conserved. Extending the theory to assume that masses of neutrinos have nonzero values and the mass eigenstates are not degenerated, a neutrino changes its flavor into another in flight. The neutrino flavor conversion is called neutrino oscillation. The neutrino oscillation was observed in the atmospheric neutrino by Super-Kamiokande (SK) [1] for the first time in 1998. Since then the neutrino oscillation parameters have been measured by reactor experiments, such as KamLAND [2], Daya Bay [3], RENO [4] and Double Chooz [5], by accelerator experiments, such as K2K [6], MINOS [7], and T2K [8], and by solar neutrino experiment, such as SNO [9], and SK [10]. However, observation of the CP violation in leptons has never been achieved so far. That is explored as the next goal of accelerator experiments such as T2K.

The neutrino oscillation happens as a quantum mechanical effect. The neutrino flavor eigenstates, $|\nu_\alpha\rangle(\alpha = e, \mu, \tau)$, are not its mass eigenstates, $|\nu_i\rangle$, but superpositions of them. The mixing of flavor eigenstates and mass eigenstates are expressed by a unitary

matrix called the Pontecorvo-Maki-Nakagawa-Sakata (PMNS) matrix [11] [12] [13], U:

$$|\nu_\alpha\rangle = \sum_i U^*_{\alpha i}|\nu_i\rangle. \tag{1.1}$$

The PMNS matrix is expressed, with ignoring the Majorana phases:

$$U = \begin{pmatrix} 1 & 0 & 0 \\ 0 & c_{23} & s_{23} \\ 0 & -s_{23} & c_{23} \end{pmatrix} \begin{pmatrix} c_{13} & 0 & s_{13}e^{-i\delta} \\ 0 & 1 & 0 \\ -s_{13}e^{i\delta} & 0 & c_{13} \end{pmatrix} \begin{pmatrix} c_{12} & s_{12} & 0 \\ -s_{12} & c_{12} & 0 \\ 0 & 0 & 1 \end{pmatrix}, \tag{1.2}$$

where $c_{ij} = \cos\theta_{ij}$ and $s_{ij} = \sin\theta_{ij}$. $\delta = \delta_{\rm CP}$ is the CP-violating phase. The probability of neutrino oscillation in vacuum is calculated, assuming ν_α with energy E is generated with charged current weak interaction, propagated for a distance L, and then detected as ν_β:

$$\begin{aligned} P(\nu_\alpha \to \nu_\beta) = \delta_{\alpha\beta} &- 4\sum_{k>j} \mathrm{Re}(U^*_{\alpha k}U_{\beta k}U_{\alpha j}U^*_{\beta j}) \sin^2\left(\frac{\Delta m^2_{kj}L}{4E}\right) \\ &+ 2\sum_{k>j} \mathrm{Im}(U^*_{\alpha k}U_{\beta k}U_{\alpha j}U^*_{\beta j}) \sin\left(\frac{\Delta m^2_{kj}L}{2E}\right), \end{aligned} \tag{1.3}$$

with differences in the squares of masses of eigenstates, $\Delta m^2_{ij} = m^2_i - m^2_j$. The muon-neutrino disappearance probability is dominated by:

$$P(\nu_\mu \to \nu_{x(\neq\mu)}) \simeq \sin^2 2\theta_{23} \sin^2\left(\frac{1.27\ \Delta m^2_{32}[\mathrm{eV}^2]\ L[\mathrm{km}]}{E_\nu[\mathrm{GeV}]}\right). \tag{1.4}$$

The dominant term of the electron-neutrino appearance is written as:

$$P(\nu_\mu \to \nu_e) \simeq \sin^2 2\theta_{13} \sin^2\theta_{23} \sin^2\left(\frac{\Delta m^2_{31}L}{4E_\nu}\right) \tag{1.5}$$

$$= \sin^2 2\theta_{13} \sin^2\theta_{23} \sin^2\left(\frac{1.27\ \Delta m^2_{31}[\mathrm{eV}^2]\ L[\mathrm{km}]}{E_\nu[\mathrm{GeV}]}\right), \tag{1.6}$$

which is common between $\nu_\mu \to \nu_e$ appearance and $\bar{\nu}_\mu \to \bar{\nu}_e$ appearance. Discovery of difference in the two oscillation probabilities of ν_e appearance and $\bar{\nu}_e$ appearance implies the CP violation in neutrino. In the framework with the PMNS matrix, the CP-violating term is dominated by:

$$\begin{aligned} &\pm \cos\theta_{13} \sin 2\theta_{13} \sin 2\theta_{12} \sin 2\theta_{23} \sin\delta \\ &\times \sin\left(\frac{\Delta m^2_{32}L}{4E_\nu}\right) \sin\left(\frac{\Delta m^2_{31}L}{4E_\nu}\right) \sin\left(\frac{\Delta m^2_{21}L}{4E_\nu}\right), \end{aligned} \tag{1.7}$$

with the $+$ $(-)$ sign for ν_e $(\bar{\nu}_e)$ appearance.

The probabilities of the neutrino oscillation, ν_e appearance and ν_μ disappearance, in the first order are plotted in Fig 1.1, where the typical parameters for T2K are used. Both probabilities have their peak at around 600 MeV. For the oscillation analysis in T2K, neutrinos around the peak energy, up to ~ 1 GeV, are important.

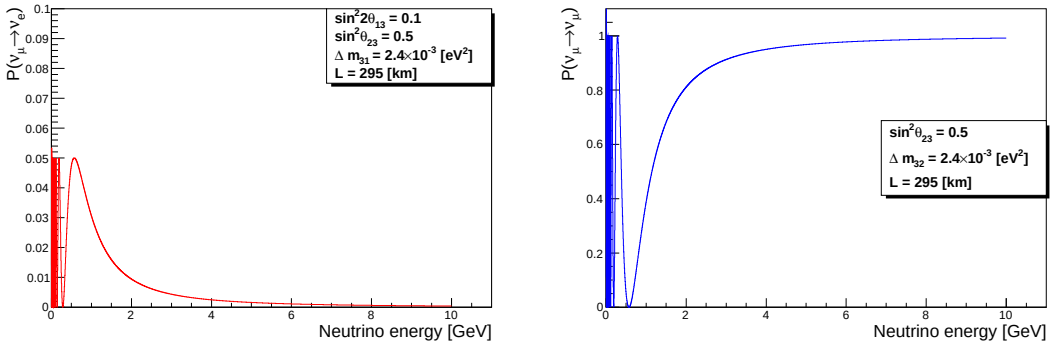

Figure 1.1: The first order probability of neutrino oscillations. Left: ν_e appearance. Right: ν_μ disappearance.

1.1.2 Neutrino masses

Observation of neutrino oscillation implies nonzero neutrino masses, but neutrino mass hierarchy is still unknown. As shown in Fig 1.2, ν_1 is the lightest in normal hierarchy, whereas ν_3 is the lightest in inverted hierarchy. At present, there is no explicit result determining the neutrino hierarchy.

The neutrino mass itself has not been measured yet, either. The best upper limits derived from laboratory experiments, such as tritium decay [14], are $m(\nu_e) < 2\,\mathrm{eV}$.

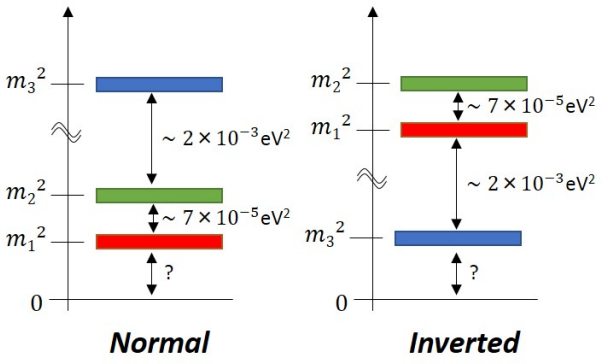

Figure 1.2: Neutrino mass hierarchy.

1.1.3 Neutrino-nucleus interaction

A neutrino interacts with a nucleon through charged current (CC) mediated by the $W^\pm$ weak bosons, or through neutral current (NC) mediated by the Z weak boson. In order to detect neutrinos and determine their flavor, charged current interactions must be used as signals. For the range of neutrino energy of T2K and WAGASCI,

up to $\sim$1 GeV, the charged current interactions are dominant as shown in Fig 1.3, in particular the charged current quasi elastic (CCQE) interaction:

$$\nu_\mu + n \to \mu^- + p, \tag{1.8}$$
$$\bar{\nu}_\mu + p \to \mu^+ + n. \tag{1.9}$$

CCQE is used as a main signal of neutrino event in these two experiments, because it is a two body scattering. The initial neutrino energy can be reconstructed by the momentum of the final charged lepton and the initial neutrino direction, assuming the target nucleon is at rest. The other modes are suppressed well by selecting neutrino energy less than 1 GeV.

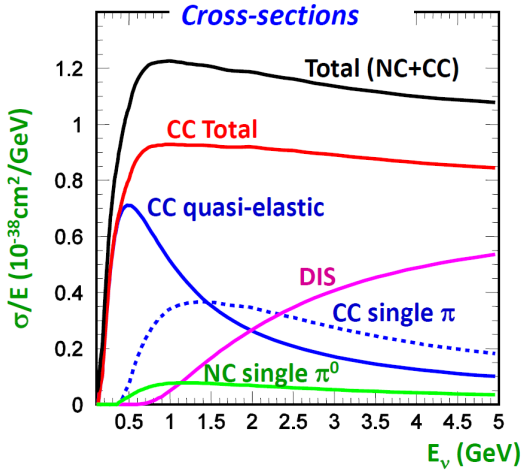

Figure 1.3: Neutrino cross sections [15]

The cross sections of CCQE are written as:

$$\frac{\mathrm{d}\sigma}{\mathrm{d}Q^2}\left(^{\nu+n\to l^-+p}_{\bar{\nu}+p\to l^++n}\right) = \left[A(Q^2) \mp B(Q^2)\frac{s-u}{M^2} + C(Q^2)\frac{(s-u)^2}{M^4}\right] \times \frac{M^4 G_f^2 \cos^2\theta_c}{8\pi E_\nu}, \tag{1.10}$$

where $Q^2 = -q^2$ and q is the four momentum transfer from the leptonic to hadronic system, M is the mass of the nucleon, θ_c is the Cabibbo angle, G_f is the Fermi coupling constant, and E_ν is the neutrino energy in the lab. s and u are the Mandelstan invariants and written as:

$$s - u = 4ME_\nu - Q^2 - m^2, \tag{1.11}$$

with the mass of the final state lepton, m. $A(Q^2)$, $B(Q^2)$, and $C(Q^2)$ describe the nucleon form factors, and are determined by neutrino-nucleon scattering experiments. The neutrino cross section depends on kinds of the target nucleus, and are described

by momentum distribution models such as the relativistic Fermi gas model and the spectral function. It is also affected by secondary interactions in nucleus. Neutrino cross sections have been measured with various targets, however, their accuracies are basically as large as 10% due to neutrino flux uncertainty. The differences between the target nucleus are expected to be small, and difficult to evaluate by the current results. In T2K oscillation analysis, for example, the difference in neutrino cross section between oxygen in water and carbon in hydrocarbon induces a large systematic uncertainty. However it is not constrained by any experimental data so far.

The charged current cross sections are different between neutrino and anti-neutrino. The cross section of neutrino is typically twice as large as that of anti-neutrino for high energy neutrinos, and about three times around 1 GeV [16]. The difference enhances contamination of neutrino background events in anti-neutrino beam, thus discrimination of anti-neutrino from neutrino is important for precise measurements of anti-neutrino cross section. The difference also implies that anti-neutrino cross section measurements require more beam flux to obtain the same statistics as neutrino measurements.

1.2 The T2K experiment

The Tokai to Kamioka (T2K) experiment, Fig 1.4, is a long-baseline neutrino oscillation experiment with the neutrino beamline in Japan Proton Accelerator Research Complex (J-PARC). The neutrino beam is measured by a near detector (ND280) located at 280 m downstream from the beam target and Super-Kamiokande (SK) at 295 km downstream. T2K adopts the off-axis method, which allows the neutrino beam to have a narrow-band flux with its peak shifted to lower energy. The 2.5° off-axis angle used in T2K gives a narrow neutrino peak around at 600 MeV as shown in Fig 1.5. Two modes of neutrino oscillation, electron neutrino appearance and muon neutrino disappearance, have been studied, and the oscillation parameters, θ_{13}, θ_{12}, and $|\Delta m^2_{32}|$, have been measured.

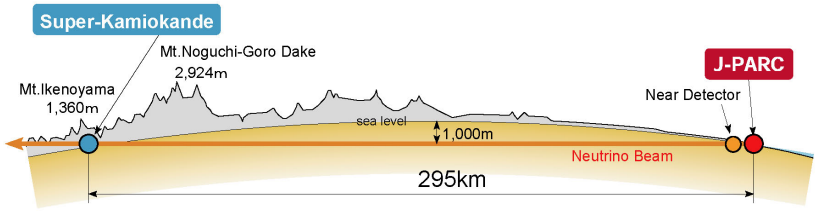

Figure 1.4: The overview of the T2K experiment.

1.2.1 The J-PARC neutrino beam

J-PARC consists of three accelerators, a linear accelerator (LINAC), a rapid-cycling synchrotron (RCS), and a main ring (MR) synchrotron. The proton beam injected into MR is accelerated up to 30 GeV. Each proton beam spill extracted to the T2K neutrino beamline from MR consists of eight bunches as shown in Fig 1.6. The protons impinges into a graphite target to produce secondary pions, which are focused by three magnetic horns and decay in flight into muons and muon-neutrinos:

$$\pi^+ \to \mu^+ + \nu_\mu, \tag{1.12}$$
$$\pi^- \to \mu^- + \bar{\nu}_\mu. \tag{1.13}$$

The neutrino beam is dominated by ν_μ when the magnetic horns are excited with 250 kA current (neutrino mode), while it is dominated by $\bar{\nu}_\mu$ with the -250 kA horn current (anti-neutrino mode). All hadrons, as well as muons below about 5 GeV/c, are stopped by the beam dump behind the pion decay volume, and neutrinos penetrate through the beam dump to be measured by the detectors.

High energy muons penetrating the beam dump are monitored by MUMON [17], a detector placed behind the beam bump, to indirectly monitor the neutrino beam direction on a spill-by-spill basis. The neutrino beam direction is also directly monitored by INGRID [18] within the required ±1 mrad during the full run period. INGRID is a detector with iron targets and placed on axis of the neutrino beam in the J-PARC site, to measure neutrino event rates and the beam direction.

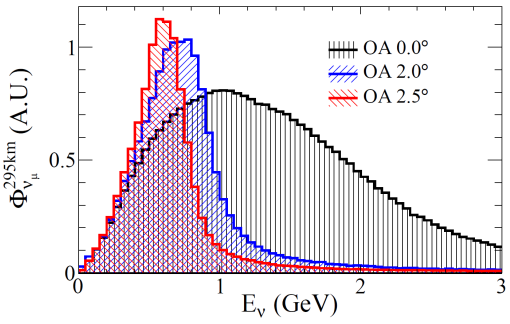

Figure 1.5: The neutrino beam flux.

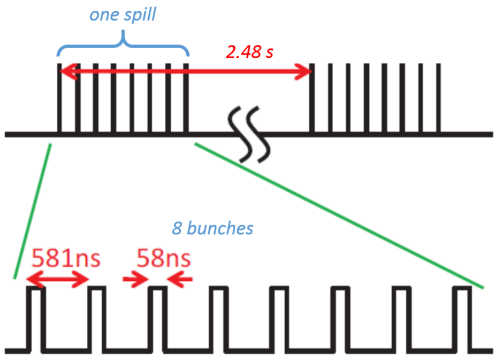

Figure 1.6: The bunch structure of the T2K neutrino beamline.

1.2.2 ND280

The ND280 detector, Fig 1.7, measures the neutrino beam in the J-PARC site at 280 m downstream from the neutrino beam target. The detectors are located on the same off-axis angle as SK, and provide constraints on the neutrino beam flux and interaction cross sections. Several detectors are put inside the magnet, and measure the

event rate of neutrino and anti-neutrino. The main neutrino target consists of hydrocarbon. The acceptance for the charged particle emitted by the neutrino interaction is mainly for forward scattering.

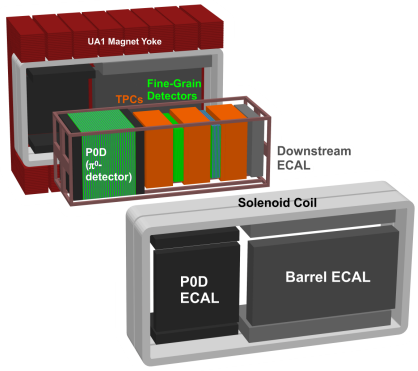

Figure 1.7: The ND280 detectors.

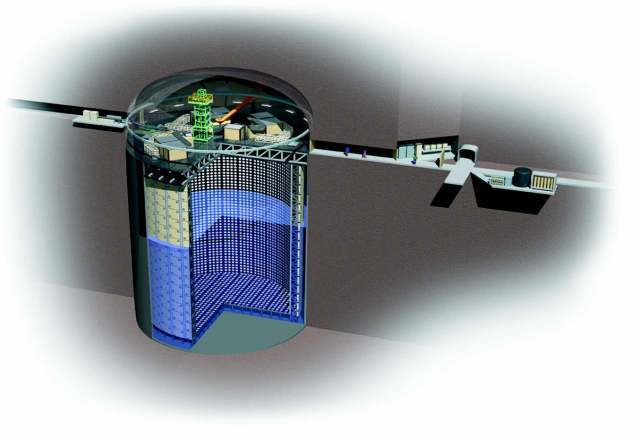

Figure 1.8: The Super-Kamiokande detector.

1.2.3 Super-Kamiokande

SK as shown in Fig 1.8 is a 50 ktons pure water detector with a cylindrical steel tank, 39.3 m in diameter and 41.4 m in height. The detector is separated into optically isolated two volumes, the inner detector (ID) and the outer detector (OD), and a large number of photomultiplier tubes (PMT) are installed on the walls inward for ID and outward for OD. The neutrino events are detected in ID by Chrenkov light of charge particles from the neutrino interactions, and discriminated from the external background by the OD veto. The ID detector is able to measure the charged particles with 4π solid angle.

1.2.4 Current status and future prospects of neutrino oscillation analysis

T2K observed electron neutrino appearance with a significance of 7.3σ [19], and the mixing parameter is measured as:

$$\sin^2 2\theta_{13} = 0.140^{+0.038}_{-0.032}\ \text{(NH)},\quad 0.170^{+0.045}_{-0.037}\ \text{(IH)}, \tag{1.14}$$

where NH means normal hierarchy and IH means inverted hierarchy. With the muon disappearance, the oscillation parameters are measured as [20]:

$$\sin^2\theta_{23} = 0.514^{+0.055}_{-0.056}\ \text{(NH)},\quad 0.511^{+0.055}_{-0.055}\ \text{(IH)}, \tag{1.15}$$

$$\Delta m^2_{32} = (2.51 \pm 0.10) \times 10^{-3}[\text{eV}^2/\text{c}^4]\ \text{(NH)},$$
$$(2.48 \pm 0.10) \times 10^{-3}[\text{eV}^2/\text{c}^4]\ \text{(IH)}. \tag{1.16}$$

Although CP-violation observation is not achieved yet, the region δ_{CP}=[0.15, 0.83]π for normal hierarchy and δ_{CP}=[-0.08, 1.09]π for inverted hierarchy are excluded, at 90% confidence level and including reactor measurements [21].

These results are obtained only with about 8% of total POT approved for T2K. Increasing the statistics and suppressing the statistical error, it becomes important to reduce the systematic uncertainties to improve the measurement precision of neutrino oscillation and to explore neutrino CP-violation.

The current systematic uncertainty for oscillation analysis is dominated by the uncertainty of neutrino cross sections in the far detector, which are not constrained by the measurement in the near detector. It is induced by the difference in the target materials between SK (water) and ND280 (hydrocarbon), and also due to the difference in acceptance, because SK has 4π acceptance whereas ND280 is mainly sensitive to forward scattering. The current total systematic uncertainties are summarized in Table 1.1. Total uncertainty for ν_e appearance is 6.8%, dominated by the independent cross sections by 4.7%, and for ν_μ disappearance is 7.7%, dominated by the independent cross sections by 5.0%. To reduce the systematic uncertainty, it is indispensable to understand better the neutrino charged current interaction with water and hydrocarbon.

Table 1.1: Relative uncertainty (1σ) on the predicted rate of ν_μ CC and ν_e CC candidate events.

Source of uncertainty	ν_μ CC	ν_e CC
Flux and common cross sections (w ND280 constraint)	2.7%	3.2%
Independent cross sections	5.0%	4.7%
SK	4.0%	2.7%
Final or secondary hadronic interaction	3.0%	2.5%
Total (w ND280 constraint)	7.7%	6.8%

1.3 Topics of this thesis

For reduction of the dominant systematic uncertainty in the T2K neutrino oscillation analysis, a new experiment at the J-PARC neutrino beamline, named WAGASCI (water grid and scintillator detector), is proposed to measure the charged current neutrino cross section ratio between water and hydrocarbon with large angular acceptance. The charged current cross section ratio measured by WAGASCI is expected to provide a correlation in the currently independent cross section parameters between the far and near detector, and to constrain the corresponding uncertainty.

The WAGASCI detector consists of two parts as shown in Fig 1.9. One is a central

detector, which contains water and hydrocarbon targets, and plastic scintillator bars. Charged particles from neutrino interactions on the targets hit the scintillators. The scintillation light is collected though wavelength shifting (WLS) fibers and detected by multi-pixel photon counters (MPPC), that is a semiconductor photon detector produced by Hamamatsu Photonics. The other part is muon range detectors (MRDs). MRDs are located at right and left sides of the central detector and at downstream. They are composed of iron layers and plastic scintillator layers, and identify muon tracks by the number of penetrated iron layers. The detail of WAGASCI will be described in Chap 2.

In this thesis, the following topics are described in the framework of the WAGASCI project. i) To reduce contamination of wrong sign neutrino events for anti-neutrino measurements, an option to install a magnetized MRD is proposed. Charge of muons from the neutrino interactions is identified by the magnetic field. The simulation method and the evaluated detector performance for the magnetized MRD are discussed in Chap 3. ii) WAGASCI will use 7760 MPPCs. Chapter 4 describes electronics used in the performance test of MPPCs before installation. iii) For synchronous readout of MPPCs to the neutrino beam bunch structure, the WAGASCI detector will use another electronics. The research and development of the new WAGASCI electronics are reported in Chap 5.

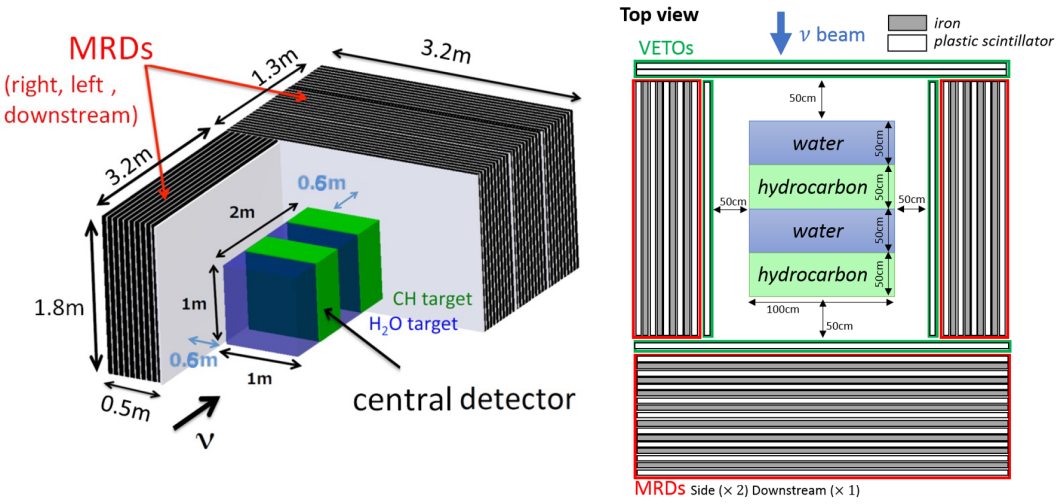

Figure 1.9: The configuration of the WAGASCI detectors.

Chapter 2

The WAGASCI experiment

WAGASCI is proposed to measure the charged current neutrino cross section ratio between water and hydrocarbon with large angular acceptance, to reduce the uncertainties in the T2K neutrino oscillation analysis. The goal of this project are:

1. to measure the charged current cross section ratio between water and hydrocarbon with 3% uncertainty,

2. to measure the charged current cross section on water and hydrocarbon individually with a large angular acceptance.

2.1 Experimental configuration

The WAGASCI detector will be located in the T2K neutrino near detector hall at J-PARC. The location of the detector will be on the 1.6° off-axis from the beam center, where we expect a similar neutrino energy spectrum to that of T2K, at 2.5° off-axis. The neutrino energy at the peak of the spectrum is around 600 MeV.

2.2 Detector design

2.2.1 The central detector

The central detector is composed of four modules, each of which contains 0.5-ton target, water or hydrocarbon, and plastic (hydrocarbon) scintillator bars. Figure 2.2 shows the side view of one of four modules. The volume of each module is $1 \times 1 \times 0.5\,\mathrm{m}^3$. The 3-mm-thick scintillator bars form the three-dimensional grid structure as shown in Fig 2.1, consisting of three different types of layers, X-layer, Y-layer, and grid-layer. Water target fills the outer vessel and the scintillator bars are sunk inside it, while hydrocarbon target fills each cell of the grid structure with cubes. This structure allows the detector to realize a large fraction of the target volume as 80%, and to have a large acceptance with almost 4π solid angle for charged particles. The total target mass is

one ton for each of water and hydrocarbon. The total number of scintillator channels in the central detector is 5120.

A neutrino in the beam interacts with a nucleus of water target or hydrocarbon by charged current interaction, and a muon is generated with other particles. Energy deposits of the charged particles on each scintillator bar are collected through WLS fibers, and the scintillation light is detected by MPPC. A track of the muon is reconstructed by the hit information in scintillators, and a vertex of the neutrino interaction is determined. Other charged particles from the neutrino interaction are also reconstructed, and used as additional information to determine the vertex. It is impossible to discriminate interactions on the scintillator bars from that on targets. This causes background events for cross section measurements, but the event rate is estimated by event rate of neutrino interactions on the hydrocarbon target.

The uncertainty of neutrino flux leads to large uncertainty in measurement of absolute cross section. It can be canceled by taking the ratio of cross section with the same neutrino flux [22]. In order to reduce the difference in neutrino flux between the water and hydrocarbon targets, these two targets are placed every 50 cm alternatively along the z axis. .

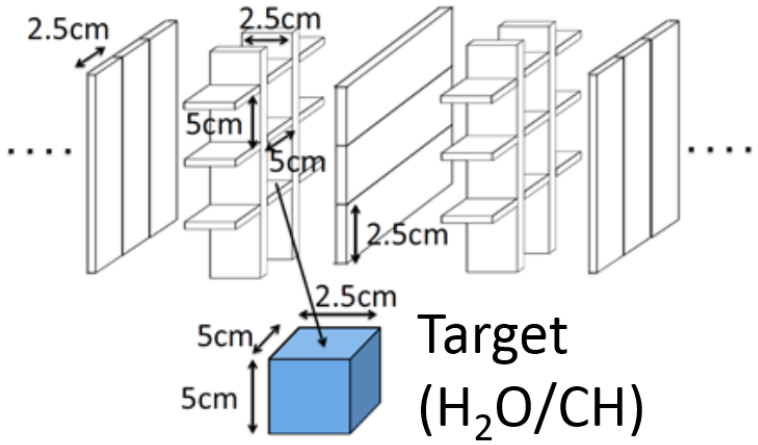

Figure 2.1: The three-dimensional grid-like structure of the plastic scintillator inside of the central detector.

2.2.2 MRDs

MRDs in the baseline design consist of iron plates and 7-mm-thick plastic scintillator bars, and form layer structures. The configuration of the downstream MRD is shown in Fig 2.3. The thickness of iron plate is 3 cm for the side MRDs and the first ten planes in the downstream MRD, and 6 cm for the last ten planes in the downstream MRD. These values are determined by requirement on the resolution of kinetic energy measurement to be 10%. The iron plates are not magnetized in the baseline design. The total mass of iron is around 49 ton (14 ton) in the downstream (side) MRD, and the total thickness

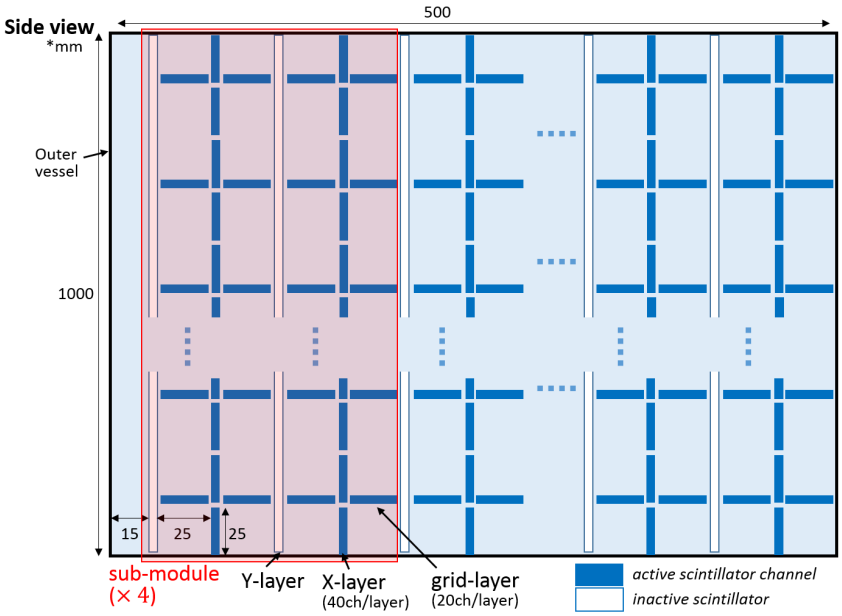

Figure 2.2: One of four modules in the central detector.

of iron is 90 cm (30 cm), to stop muons with energy less than 1 GeV. The scintillator bars are arranged only vertically with segmentation of 20 cm. Two MPPCs readout a scintillator bar at both sides with a WLS fiber, and their time difference provides information of position along y axis with around 10 cm precision. Total number of readout channels in the MRDs is 1280, taking into account the double readout.

Neutrino charged current interactions on the target in the central detector are identified by reconstructing a track of muon. Tracks of other charged particles are rejected by requiring a threshold for the number of iron planes penetrated in the MRDs.

2.2.3 Vetos

The MRDs are placed at 50 cm away from the central detector, and the veto layers are put on the inward surface of MRDs and the upstream end of the WAGASCI detector. The veto layers consist of horizontal and vertical scintillator bars, and the total number of channels is 1360.

One of major background in neutrino interaction events of WAGASCI is due to particles generated in interaction outside the detector or in MRDs which enter into the central detector. Such external background events are rejected by measuring timing difference between hits in the central detector and in the veto layers.

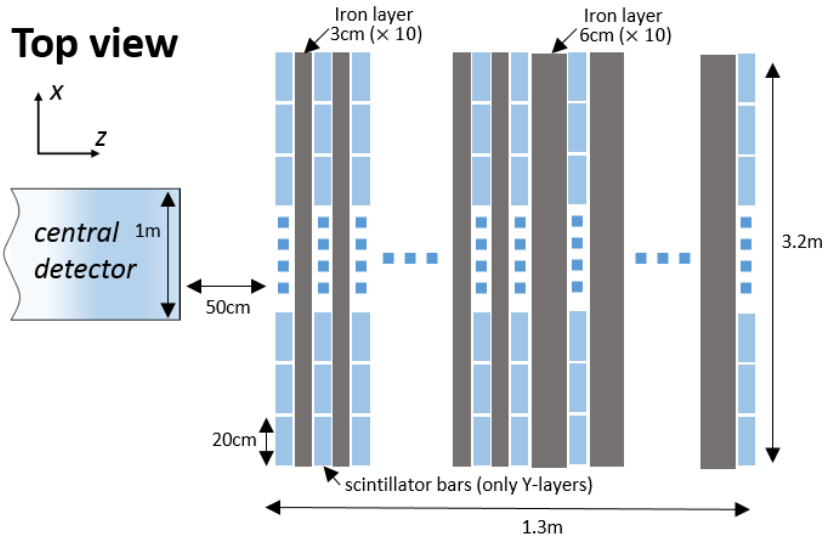

Figure 2.3: Configuration of the downstream MRD.

2.3 Expected performance

The performance of the detector is evaluated by Monte Carlo simulation for the neutrino mode beam [23]. As the event selection for the cross section measurement, the tracks of charged particles are required to penetrate 3(15)-cm-thick iron plates in side (downstream) MRDs, in order to reduce the background from other charged particles than muons. Tracks are required to stop within the MRDs, or to penetrate through all planes of an MRD. Table 2.1 shows the expected number of events from the 1-ton hydrocarbon target and 1-ton water target with 10^{21} Protons On Target. The number of charged current interactions after the event selection is expected to be 3×10^4 events with 92% purity for hydrocarbon. The purity is worse for water target because of the background from interactions on the scintillators in the central detector, but that background is constrained by event rate on hydrocarbon target. The cross section ratio between water and hydrocarbon is expected to be measured with a total uncertainty of 3%.

2.4 Option to magnetized the downstream MRD

The half of the neutrino beam for T2K will be operated with the anti-neutrino mode, and the WAGASCI detector will also be exposed to it. The anti-neutrino beam at J-PARC has more contamination of the wrong sign neutrino background than that with the neutrino beam. Taking into account the cross section of neutrino charged current interaction with a nucleus is about three times larger than that of anti-neutrino, about 30% of all the charged current interactions in the WAGASCI detector are expected to

Table 2.1: The expected number of neutrino events in the WAGASCI detector after all event selection for the neutrino beam with 10^{21}POT.

	CC	NC	BG from outside	BG from scintillators	Total
hydrocarbon (1 ton)					
Events [/10^{21}POT]	3.0×10^4	1.2×10^3	1.6×10^3		3.3×10^4
Fraction	91.7%	3.5%	4.8%		100%
water (1 ton)					
Events [/10^{21}POT]	2.4×10^4	0.9×10^3	1.6×10^3	6.2×10^3	3.3×10^4
Fraction	73.5%	2.6%	5.0%	18.9%	100%

come from the wrong sign background. Thus, discrimination of anti-neutrino events from neutrino event is indispensable for the precise measurement of the anti-neutrino cross section.

To reduce the contamination of neutrino backgrounds in anti-neutrino measurements, an option is proposed to install an MRD with magnetized iron at the downstream of the central detector instead of the current downstream MRD without magnetic field as described in Sec 2.2.2. The sign of particle charge from the (anti-)neutrino interaction is identified by the bending direction in the magnetic field.

2.5 Electronics for the WAGASCI experiment

2.5.1 Electronics for the MPPC mass test

For the WAGASCI detector, a new 32-channel arrayed MPPC, as shown in Fig 2.4, is developed. It has low dark noise rate and after-pulsing rate, wider range of operation voltage ($\sim$5 V), and low crosstalk rate. WAGASCI uses 7760 channels of MPPCs in total.

The performance of all the MPPCs, such as the dark noise rate, crosstalk rate, gain, and photon detection efficiency, will be measured before installation into the detectors. In the mass test, the readout and control, such as amplification of the waveform and bias voltage adjustment, are required for a large number of MPPCs at the same time. As front-end readout electronics, an Extended Analogue SI-pm ReadOut Chip (EASIROC) is adopted. EASIROC, developed by OMEGA/IN2P3 [24], is a 32 channels fully analogue front end ASIC dedicated to readout SiPM detectors, and does not include digital signal processing. A NIM module with EASIROC will be used in the mass test, after the firmware on the module to control EASIROC is updated to include such functions as a scaler required to count the signal rate.

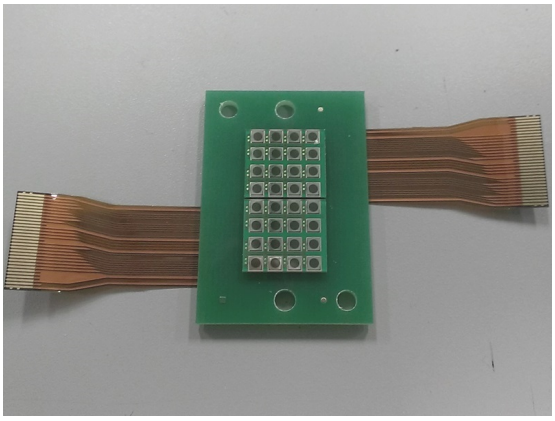

Figure 2.4: The front side of 32-channel arrayed MPPC.

2.5.2 Electronics for the signal readout in WAGASCI

Signals from all the MPPCs in WAGASCI are required to be readout synchronously to the bunch structure of the J-PARC neutrino beam. Controls of all the MPPCs, such as bias adjustments, must be done at the same time. As front-end electronics of the WAGASCI detector, a Silicon PM Integrated Read-Out Chip (SPIROC) is adopted. SPIROC is a 36-channel auto-triggered front-end ASIC, and is produced by OMEGA/IN2P3 too. The functionality of analog parts in SPIROC is studied with the EASIROC chip, which only contains the analog functions simplified from SPIROC. SPIROC also contains the digital parts such as auto-trigger and timing measurement.

New readout electronics for the WAGASCI detector are under development with the SPIROC2D chip, which is the latest version of SPIROC. Each readout board is designed to control a 32-channel arrayed MPPC, and 256 SPIROC2D chips are planned to be used.

2.6 Schedule

WAGASCI is approved as a test experiment, J-PARC T59. The design of the detector and R&D of the detector components are ongoing. The construction and installation of the WAGASCI detector will be done at August 2016 and the physics operation will start at the autumn 2016.

Chapter 3

Simulation study of magnetized downstream muon range detector

For discrimination of anti-neutrino events from neutrino events in the WAGASCI detector with the anti-neutrino beam, it is proposed to use a magnetized MRD constructed in Baby-MIND [25] at downstream of WAGASCI. Baby-MIND, a project independent of WAGASCI, could provide a magnet system and an MRD composed of the magnetized steel plates and scintillator bars. Optimization of the configuration of the magnetized downstream MRD is still going on to achieve the precise measurement of anti-neutrino cross section ratio between water and plastic with 3%, as the same accuracy for the ν_μ cross section measurement.

The performance of the WAGASCI detector with the magnetized downstream MRD, such as track reconstruction, muon discrimination from the other charged particles, and charge identification, is evaluated with Monte Carlo simulation. In this chapter, the current configuration of the magnetized downstream MRD, the framework of analysis method, and the expected performance with the Monte Carlo simulation will be discussed.

3.1 Contamination of wrong sign neutrino.

3.1.1 Neutrino flux

The J-PARC anti-neutrino beam mainly contains anti-muon-neutrino ($\bar{\nu}_\mu$), but the fraction of muon-neutrino (ν_μ) is not negligible. The fraction of the other components, such as electron-neutrino (ν_e) and anti-electron-neutrino ($\bar{\nu}_e$), is about 1% [23]. The following study does not include the electron-type components, and only considers ν_μ and $\bar{\nu}_\mu$. Contamination of the wrong sign neutrino in the anti-neutrino beam mode is larger than that of the neutrino mode. For the comparison between these two neutrino modes, the neutrino beam flux is predicted by simulation with JNUBEAM [26], which is a simulation tool for the T2K neutrino beam line. In JNUBEAM collisions of primary proton beam with a graphite target are simulated, and secondaries are focused by

magnetic horns. Sequential decays of the secondaries into neutrino are simulated, and the fluxes and energy spectrum are provided for each neutrino flavor.

The fluxes are shown for both of neutrino and anti-neutrino modes in Fig 3.1. The integrated neutrino flux of ν_μ and $\bar{\nu}_\mu$ at the place of the WAGASCI central detector is $2.87 \times 10^{13}/\mathrm{cm}^2/\ 10^{21}$ POT for the neutrino mode, and $2.30 \times 10^{13}/\mathrm{cm}^2/10^{21}$ POT for the anti-neutrino mode. The fractions of ν_μ and $\bar{\nu}_\mu$ in the beam flux are summarized in Tables 3.1 and 3.2. The flux with the neutrino beam mode is 94.9% μ_ν, while that with the anti-neutrino mode is 91.6% $\bar{\nu}_\mu$. The contamination of the wrong sign neutrino is expected to be 5.1% (8.4%) with the neutrino (anti-neutrino) mode.

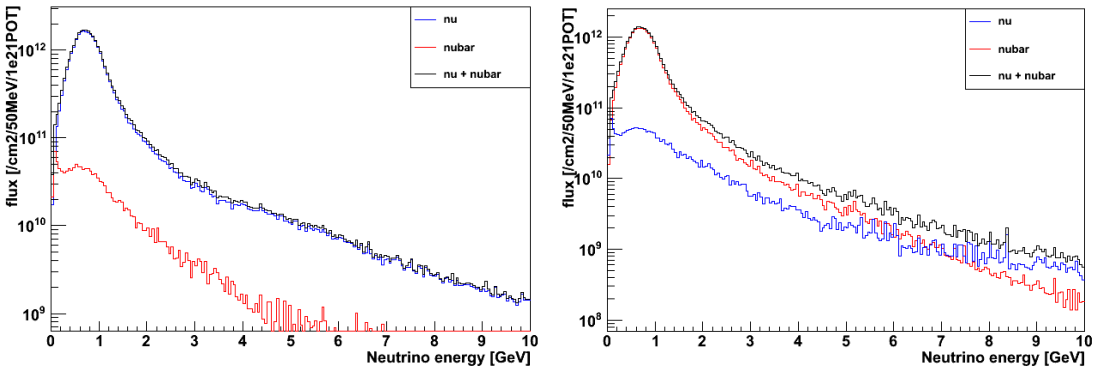

Figure 3.1: The J-PARC neutrino beam flux predicted by JNUBEAM at the WAGASCI detector. Left: neutrino mode. Right: anti-neutrino mode.

Table 3.1: Flux components of the neutrino mode beam.

	0 - 2 GeV	All
ν_μ	2.51×10^{13} (95.3%)	2.72×10^{13} (94.9%)
$\bar{\nu}_\mu$	1.23×10^{12} (4.7%)	1.45×10^{12} (5.1%)
Total	2.63×10^{13} (100%)	2.87×10^{13} (100%)

Table 3.2: Flux components of the anti-neutrino mode beam.

	0 - 2 GeV	All
ν_μ	1.44×10^{12} (6.7%)	1.93×10^{12} (8.4%)
$\bar{\nu}_\mu$	2.01×10^{13} (93.3%)	2.11×10^{13} (91.6%)
Total	2.15×10^{13} (100%)	2.30×10^{13} (100%)

3.1.2 Neutrino interaction

Charged current neutrino interactions at the WAGASCI central detector are predicted by simulation with NEUT [27], which predicts neutrino interactions with a target nucleon and behavior of secondary particles within the target nucleus. It provides the neutrino interaction rate and kinematics of the particles from the neutrino interaction by using the neutrino flux information predicted with JNUBEAM.

The neutrino interaction rates as a function of neutrino energy are shown in Fig 3.2. Two tons of water with the volume of $1{\times}1{\times}2\,\mathrm{m}^3$ are assumed as a target. The numbers of interactions are summarized in Tables 3.3 and 3.4. Although the contamination from the wrong sign neutrino with the neutrino beam is 2%, that with the anti-neutrino beam is 32%. Thus, discrimination of the neutrino and anti-neutrino is indispensable in order to measure the anti-neutrino cross section with high precision.

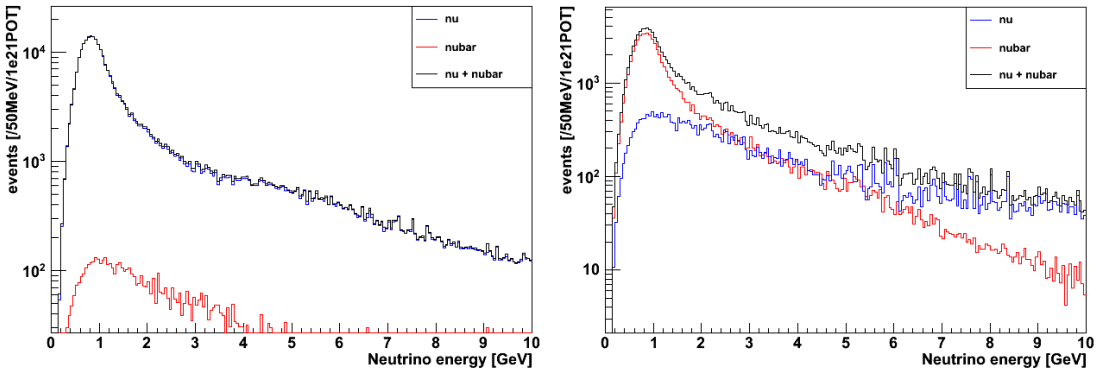

Figure 3.2: The charged current interactions in the WAGASCI central detector predicted by NEUT. Left: neutrino mode. Right: anti-neutrino mode.

Table 3.3: The charged current interactions in the central detector with the neutrino mode beam.

	0 - 2GeV	All
ν_μ	$2.14{\times}10^5$ (98.5%)	$2.99{\times}10^5$ (97.8%)
$\bar{\nu}_\mu$	$3.28{\times}10^3$ (1.5%)	$6.65{\times}10^3$ (2.2%)
Total	$2.17{\times}10^5$ (100%)	$3.06{\times}10^5$ (100%)

3.1.3 Muon distribution

Figure 3.3 shows distributions of the muon angles from the neutrino beam axis and contamination of wrong sign events, for the (anti-)neutirno interactions in the central detector with the anti-neutrino beam. Table 3.5 summarizes the number of events for the scattering angles of 0° to 30°, 30° to 60°, and 60° to 90°. The fraction of contamination is around 30%, except for muons emitted very forward with the 40%

Table 3.4: The charged current interactions in the central detector with the anti-neutrino mode beam.

	0 - 2GeV	All
ν_μ	1.24×10^4 (18.8%)	3.28×10^4 (32.4%)
$\bar{\nu}_\mu$	5.37×10^4 (81.2%)	6.85×10^4 (67.6%)
Total	6.61×10^4 (100%)	1.01×10^5 (100%)

contamination. The large fraction of the muons is emitted forward to the downstream direction, hence the reduction of contamination is more important in the downstream MRD than that in the side MRDs.

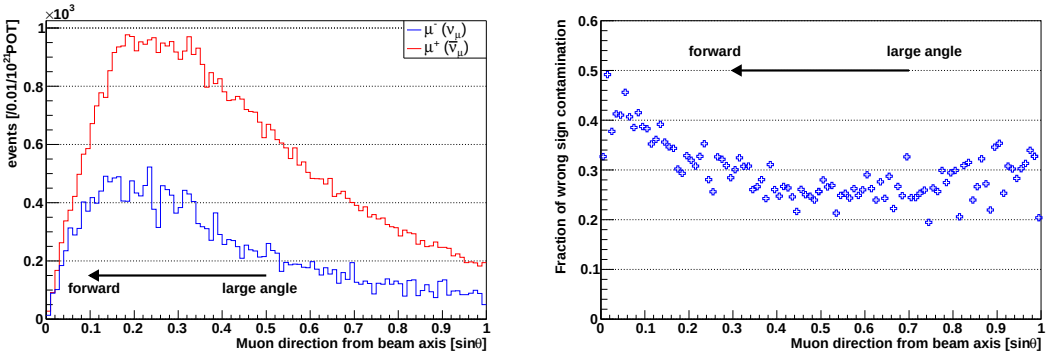

Figure 3.3: Muon distributions in WAGASCI for the anti-neutrino beam. Left: Angular distribution. Right: The fraction of wrong sign contamination.

Table 3.5: The number of muon events and the fraction of the wrong sign contamination.

	0° - 30° (Downstream	30° - 60° - - - - - - -	60° - 90° Large angle)
μ^- (ν_μ)	1.7×10^4 (31.3%)	5.6×10^3 (26.2%)	1.2×10^3 (29.6%)
μ^+ ($\bar{\nu}_\mu$)	3.7×10^4 (68.7%)	1.6×10^4 (73.8%)	2.9×10^3 (70.4%)
Total	5.4×10^4 (100%)	2.1×10^4 (100%)	4.1×10^3 (100%)

3.2 Requirements for the magnetized downstream MRD

In order for the magnetized downstream MRD to be a feasible option, it is required to keep the ability as an MRD with the same performance as the current non-magnetized design [23], while reducing the wrong sign neutrino contamination in anti-neutrino mea-

surement down to the same level as that in neutrino measurement. Hence, requirements on the magnetized downstream MRD are:

- To discriminate muons from all the other charged particles such as charged pions and protons by requiring to penetrate the iron plates, with purity of more than 90%.
- To measure kinetic energy of the muons by the number of the penetrated iron plate with 10% accuracy.
- To identify the charge sign of particles by the bending direction in the magnetic field with efficiency of 90%, for a reduction of the wrong sign contamination down to about 2%.

3.3 Concept of the magnetized downstream MRD

The concept of the magnetized downstream MRD is shown in Fig 3.4. It consists of a layer structure with magnetized steel plates and scintillator planes. The scintillator planes are composed of plastic scintillator bars arranged vertically and horizontally, and provides the position information of hits of charged particles. Tracks of the charged particles are reconstructed by using the hit information.

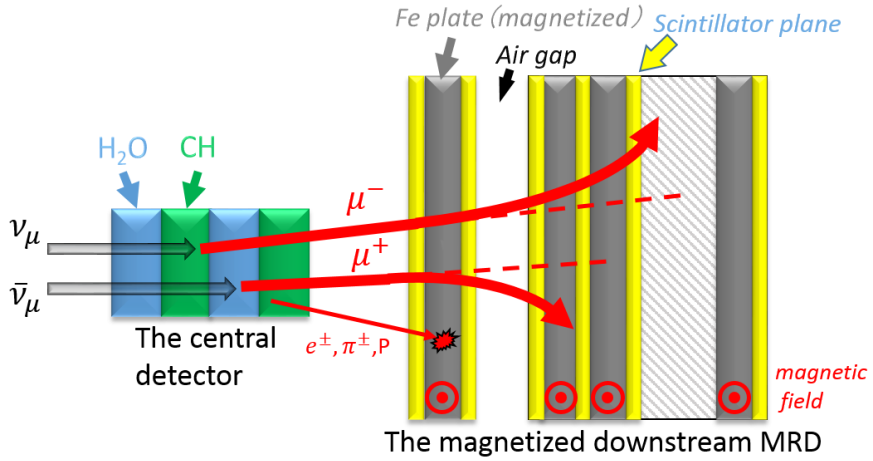

Figure 3.4: The overview of the central detector and magnetized downstream MRD.

3.3.1 Muon discrimination

Figure 3.5 shows kinetic energy distributions for muons, charged pions, and protons from anti-neutrino interactions in the central detector. The kinetic energy of muons is higher than that of the other charged particles. In addition, range of muons is longer than that of the other particles at the same kinetic energy, as calculated in

Appendix A. Thus, muons can be discriminated from the other charged particles by requiring to penetrate the first iron plate, if the thickness is determined to be large enough.

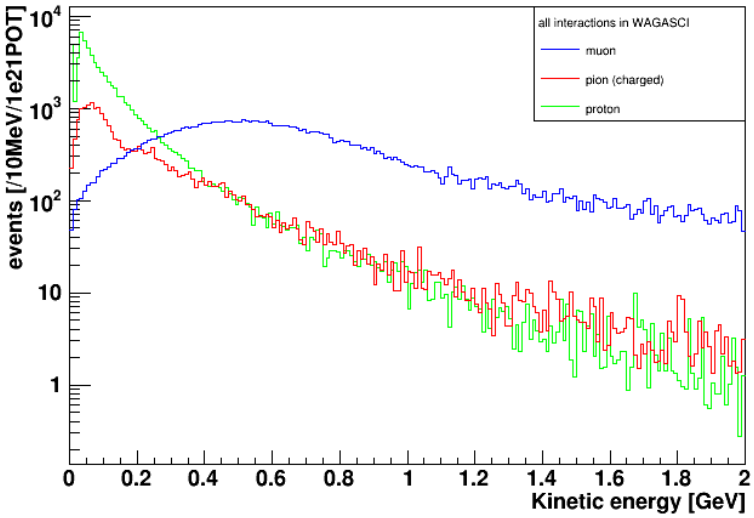

Figure 3.5: Kinetic energy distribution of muon, charged pion, and proton from the $\bar{\nu}_\mu$ interactions in the central detector.

3.3.2 Kinetic energy measurement

The path length of a muon in material, mainly iron, is calculated by the number of the penetrated iron plate, taking into account the reconstructed vertex position and angle of track. It provides information of kinetic energy of the muon, estimating electric energy loss in the material.

The track of muon is bent by the magnetic field, and the bend might provide the momentum information because the bending radius is in proportion to the momentum. However, multiple coulomb scattering in iron is large and changes the bend direction randomly. Measuring the momentum of muons by the bend in the magnetic field is not promising, nor used in the following study.

3.3.3 Charge identification

The track bend of muons from (anti-)neutrino interactions is measured in the magnetized downstream MRD with two different method: i) fitting the track with a quadratic function and ii) measuring the angle difference before and after the first iron plate. Either way, multiple coulomb scattering in iron randomly involves the track bend and decreases efficiency of the charge identification. In order to enhance resolution in the track angle, the air gap is put after the first iron plate.

3.4 Current configuration of the magnetized downstream MRD

3.4.1 Magnetized steel plate

Figure 3.6 shows the current design of a magnetized steel plate. It consists of a $3.5 \times 2.0\,\mathrm{m}^2$ steel plate with a one-cm slit at the center separating itself into two parts, and 4-mm aluminum coils wound around the top and bottom parts on each individual plate. The magnetic field is produced inside the steel plate by the normal conducting coils. The calculated magnetic field is shown in Fig 3.7. For the wide region of the steel plate, the magnetic field is uniformly 1.5 tesla. The slight ununiformity of the magnetic field will be solved in the next version of magnetized steel plate. It contains two 1-cm slits and the magnetic field goes round back with two loops as shown in Fig 3.8.

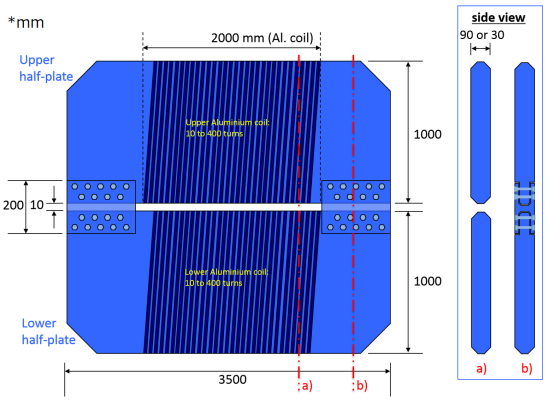

Figure 3.6: The design of magnetized steel plate with a single slit.

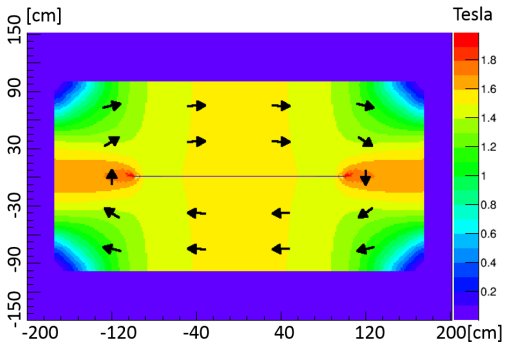

Figure 3.7: The map of the simulated magnetic field.

For charge identification the central part of the steel plate where the magnetic field runs horizontally is mainly used, and charged particles are bent along the vertical axis. The simulation study has only been done with the single-slit magnetized steel plate so far. The analysis methods for the single-slit version described below are applicable with small modification to the double-slit one, too. The performance as an MRD is expected to be the same between the two versions. The double-slit version is expected to have better the charge identification ability because of its widely uniform magnetic field.

3.4.2 Scintillator module

The scintillator module is currently designed as Fig 3.9 for the single-slit magnetized steel plate. In order to obtain high resolution of track directions along the vertical axis, segmentation of the horizontal bars is finer than that of the vertical bars. The 3-cm-wide horizontal bars compose two layers staggered with each other. This structure enables

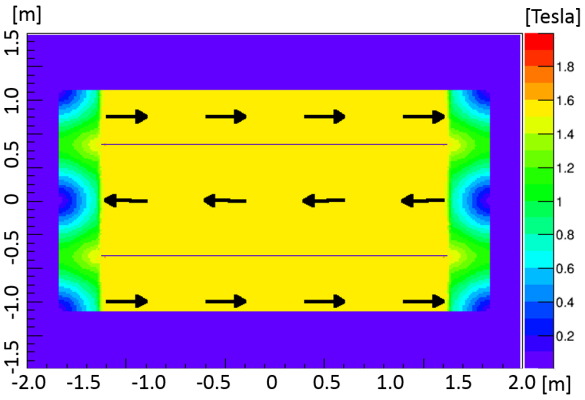

Figure 3.8: The map of the simulated magnetic field map with double slits.

to have a segmentation of 1.5 cm and to compensate slight spaces between the bars for each other layer. For the vertical scintillator bars 10-cm coarse segmentation is selected at the middle part. 3-cm segmentation is kept at the outer parts, and allows to measure the bend direction of tracks along the horizontal axis. This is required for the single-slit magnetized steel plate because the magnetic field contains some vertical components at the outer part. However, it will not be required any more for the double-slit version because the region with vertical magnetic field becomes much smaller.

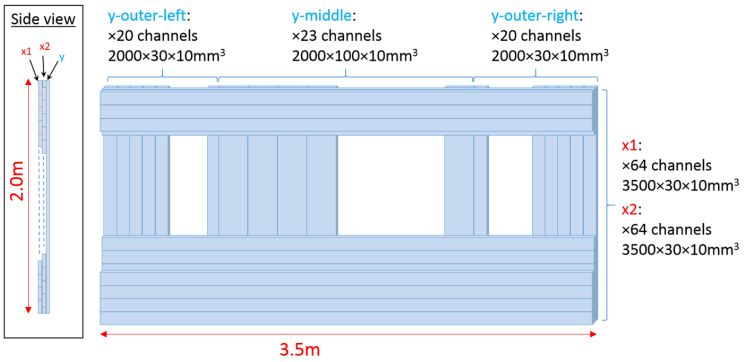

Figure 3.9: The scintillator module composed of plastic scintillator bars.

3.4.3 Downstream MRD

The current configuration of the magnetized downstream MRD is shown in Fig 3.10. It is constructed with a layer structure of the scintillator modules and the single-slit magnetized steel plates. The thickness of the first steel plate (m1) is chosen as 9 cm taking into account the charge identification and non-muon particle rejection capabili-

ties (for the detail see Appendix A). The thickness of the other plates, except for the most downstream plate, is determined to be 3 cm to obtain the same minimum segmentation for muon range measurement as the current WAGASCI MRD. To simplify the production procedure, the 27 steel plates in the middle are designed to have the same thickness, and some plates are combined where a coarse segmentation is sufficient, as shown in Fig 3.10. The most downstream plate (m29) has 9-cm thickness to adjust the total iron thickness. Total thickness of iron in the downstream MRD is 99 cm to stop muons with energy less than 2 GeV.

The distance between the first scintillator module (s0) and the second one (s1) is kept 50 cm to measure time of flight of charged particles and to decrease external backgrounds [23]. There are two more air gaps between scintillator modules (between s2 and s3, and s4 and s5) in order to obtain higher resolution in the angle measurement.

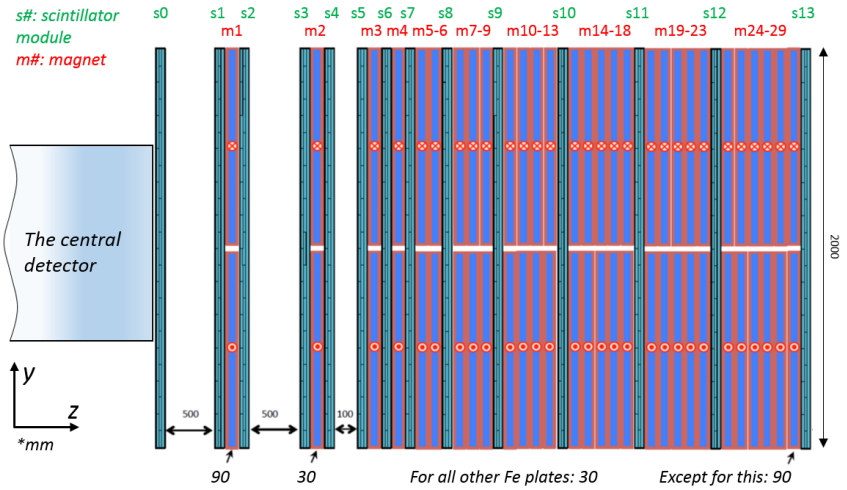

Figure 3.10: The current configuration of the magnetized downstream MRD.

3.5 Framework of the Monte Carlo simulation

The procedure of the Monte Carlo simulation to evaluate the performance of the WAGASCI central detector and the magnetized downstream MRD is described.

3.5.1 Detector configuration

The central detector is simplified and consists of two tons of water target and the three-dimensional grid structure of scintillator bars. Although the detector is designed with one-ton water and one-ton hydrocarbon as explained in Sec 2.2.1, the densities of water and hydrocarbon are different only by about 3% and does not significantly affect

the study of charge identification.

The magnetized downstream MRD is constructed with the current design as shown in Fig 3.10. It is composed of just the magnetized steel plates and scintillator modules. The magnetic field is only distributed inside the steel and uniform along the z axis. The aluminum coils are not taken into account. The side MRDs and veto planes are not included.

3.5.2 Event generation

Neutrino flux generation and neutrino interaction are simulated with JNUBEAM and NEUT, respectively. The WAGASCI detector response is simulated by GEANT4-based detector simulation [28] [29] [30] [31].

1. Events of the neutrino interactions are generated with the predicted flux with 10^{21} POT. Neutrino interactions are distributed within the water target uniformly along the beam direction, and particles from the neutrino interaction are generated in the central detector.

2. Hit information on the plastic scintillator bars are stored if there are any energy deposit of the charged particle. Any other effects are not included so far, such as scintillator saturation (Birks' saturation), light collection efficiency, attenuation in the scintillator bar or WLS fiber, and response of MPPC and electronics.

Figure 3.11 shows an event display of $\bar{\nu}_\mu$ CCQE interaction. A positive muon and a neutron are emitted. The positive muon is bent by the magnetic field at the downstream MRD, and stops between the 9th and 10th scintillator layers.

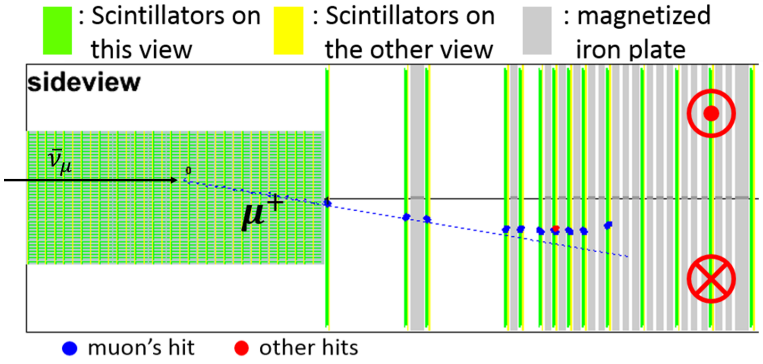

Figure 3.11: Event display of a CCQE event with $\bar{\nu}_\mu$. The blue-dotted line is the initial direction of μ^+.

3.5.3 Track reconstruction

The track reconstruction is done by using the cellular automation method [32]. It is already confirmed that the method correctly reconstructs muon tracks from neutrino

interactions with a detector composed of layer structure of iron plates and plastic scintillator bars [33] [34]. In order to reconstruct curved tracks in the magnetized downstream MRD, the method is slightly modified. The procedure is described in the followings.

Linear track reconstruction (Fig 3.12)

For the whole region of the central detector and for the four-separated regions in the downstream MRD, linear tracks are reconstructed on each of side view and top view by using the cellular automation method. In the central detector, only the scintillator bars on x-y layers are taken into account and those on grid-parts are not, because tracks with a large angle are not relevant for the study with the downstream MRD.

Connection of the linear tracks (Fig 3.13)

1. A pair of tracks can be a candidate to be connected together if their position difference along x (y) axis is smaller than 200 mm at the joint for top (side) view.

2. A track in the central detector and a track at the most upstream in the downstream MRD are connected first. The angular difference projected on the current view must be smaller than 35 degrees.

3. The track is extended toward downstream if there is another track to be connected. The angular difference on the current view must be smaller than 50 degrees.

4. If there are more than one candidate to be connected, a track with the smallest difference in the angle is selected.

5. Only tracks passing through the fourth scintillator plane (s3 in Fig 3.10) are selected as muon tracks.

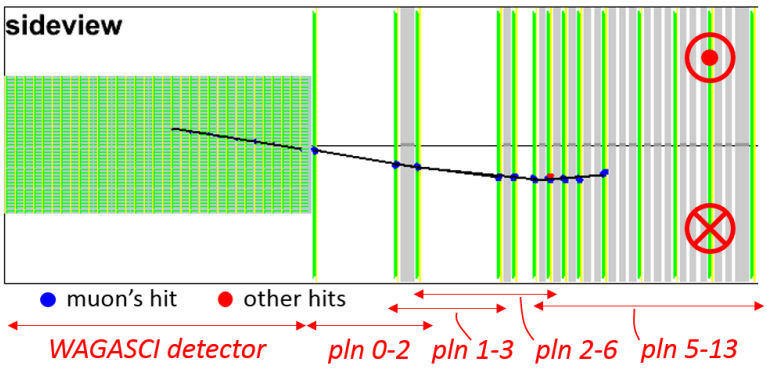

Figure 3.12: Event display of track reconstruction in each view and in each region.

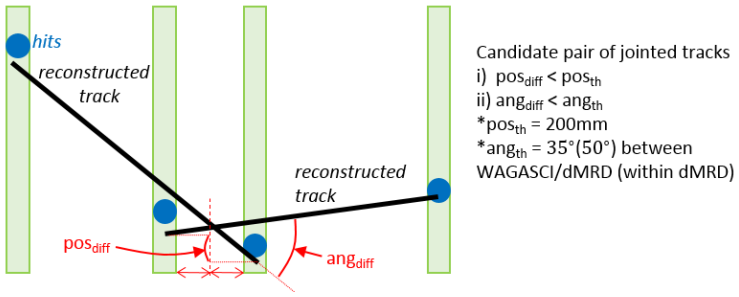

Figure 3.13: Candidate pair of tracks to be joined to each other.

Three-dimensional track reconstruction

A pair of tracks in top view and side view is selected. If there are more than one pair of tracks, the pair with smallest difference in the positions of initial points and end points is taken as the three-dimensional reconstructed track.

Stop in MRD

The end point of the track must be at least 10 cm away from the MRD's surface, in order to remove tracks going out from the side surface of the downstream MRD. It is also required that there is no hit on the most downstream scintillator layer.

Fiducial volume cut

The track initial point must be at least 5 cm away from the central detector's surface, in order to avoid selecting external charged particles in real experiment.

3.5.4 Charge identification

In order to improve the performance of charge identification, two different methods are considered.

Fitting with a quadratic function (Fig 3.14)

All the hits in the reconstructed track in the downstream MRD are fitted with a quadratic function ($ax^2 + b + c$). The bend direction is measured by the second order coefficient (a), and its sign provides the information of the charge sign. It is also taken into account whether the track runs in top region or bottom, because the direction of magnetic field is opposite. If the track crosses the middle horizontal plain, $y = 0$, the bend direction is changed. In this case the longest part of the track in either top region or bottom is analyzed and the other parts are ignored.

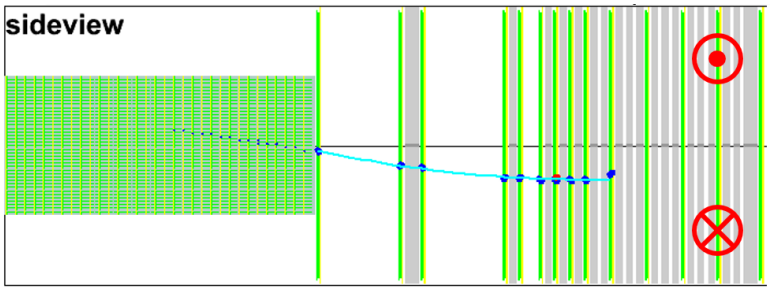

Figure 3.14: Event display of fitting with a quadratic function.

Angular difference measurement at the first steel plate (Fig 3.15)

For short tracks, it might become harder to fit with a quadratic function. In that case, the angular difference is measured between the initial and final directions at one steel plate. The two large air gaps enable to obtain higher resolution of angle. In this study, however, only the fitting method above has been used and this angular difference measurement has not been studied so far.

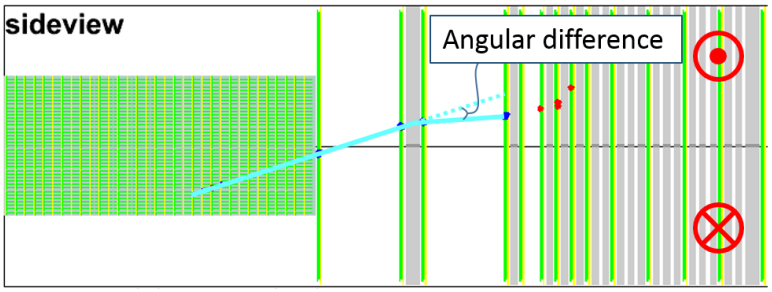

Figure 3.15: Event display of angular difference measurement.

3.6 Expected performance of the magnetized downstream MRD

3.6.1 Track reconstruction efficiency

Although the track reconstruction procedure explained in Sec 3.5.3 can be optimized more, for example by adjusting each parameter and/or how to separate regions, the reconstruction efficiency is already expected to be good enough. Figure 3.16 shows three kinetic energy distributions: i) for muons passing through the fourth scintillator plane in the downstream MRD, ii) in addition after the fiducial volume cut requiring the generated position to be at least 5 cm away from the central detector surface, iii) and for all the reconstructed muon tracks without requiring to stop in the MRD. The ratio of the number of reconstructed muon tracks to the number of muons after the

fiducial volume cut is 90.1%.

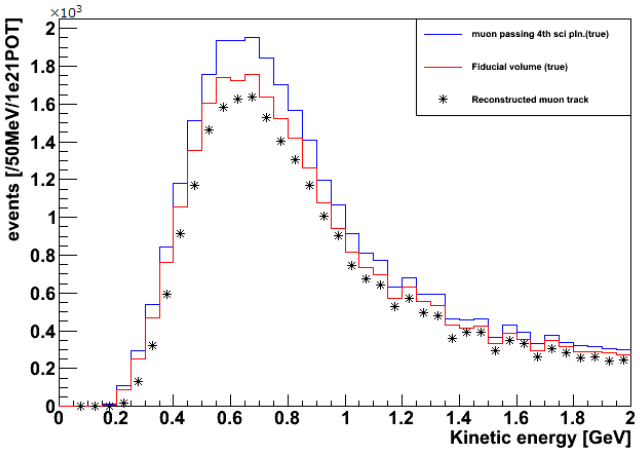

Figure 3.16: Muon's kinetic energy distribution. Blue line: Muons passing the 4th scintillator plane. Red line: Fiducial volume cut is added. Points: The reconstructed muon tracks.

3.6.2 Event selection

Figure 3.17 shows muon kinetic energy distribution for each procedure of the analysis. From all the reconstructed tracks with the central detector and the downstream MRD, the tracks are required to stop within the downstream MRD. Charge identification selection as described in Sec 3.6.4 is done for the tracks stopping in the MRD.

Table 3.6 shows the number of muons. A large amount of positive muons with energy more than 2 GeV for the anti-neutrino events are removed by requiring to stop in the MRD and their fraction goes down to 1.5%, while 15% of the negative muons from neutrino events remains. The positive muons are bent inward to the middle plane ($y = 0$), whereas the negative muons are bent outward to the side surfaces. Hence, some high energy tracks going out of the side surfaces still remain because of their large angle, even after removing tracks ending at close to the side surfaces.

Table 3.6: The number of muons and fraction of muons stopping in the MRD.

		0-1 GeV	1-2 GeV	2-5 GeV
nu	All tracks	2030	3363	4524
	Stop in MRD	1108 (54.6%)	1369 (40.7%)	686 (15.2%)
nubar	All tracks	16791	8128	5626
	Stop in MRD	12073 (71.9%)	4086 (50.3%)	85 (1.5%)

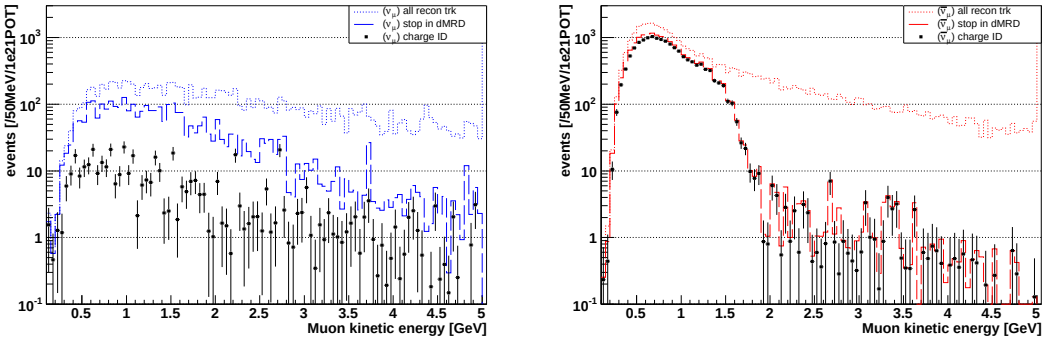

Figure 3.17: Event selections (Left: ν_μ, Right: $\bar{\nu}_\mu$). Dotted line: All reconstructed tracks. Broken line: Stop in the downstream MRD. Points: Charge identification.

3.6.3 Purity of muons

The distributions of the reconstructed tracks stopping in the MRD for μ^+, $\pi^\pm$, proton, and $e^\pm$ are shown in Fig 3.18. This is before charge identification. The purity of muon track is 97% (Table 3.7), and the charged current neutrino interactions are extracted well.

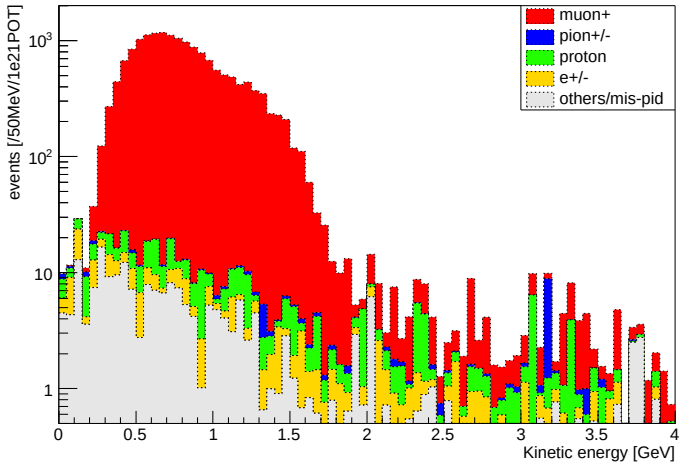

Figure 3.18: Kinetic energy distribution of reconstructed tracks stopping in the downstream MRD.

3.6.4 Charge identification

The charge identification reduces the wrong sign event (ν_μ) well after the selection of stopping tracks in the MRD. Figure 3.19 (left) shows the distribution of the parameter

Table 3.7: Components of reconstructed tracks stopping in the downstream MRD.

μ^+	$\pi^\pm$	proton	$e^\pm$	others/mis-ID	All
16261	30	178	110	218	16797
96.8%	0.2%	1.1%	0.7%	1.3%	100%

used to identify the sign of charge. That is the coefficient in the second order of the quadratic function fitting charged particle track, multiplied by +1 (−1) when the track runs in the bottom (top) region. The distribution of the $\bar{\nu}_\mu$ events are shifted toward positive, and that of ν_μ is shifted toward negative. Defining a threshold value for that charge identification parameter, $\bar{\nu}_\mu$ events are selected as the events with the parameter more than the threshold.

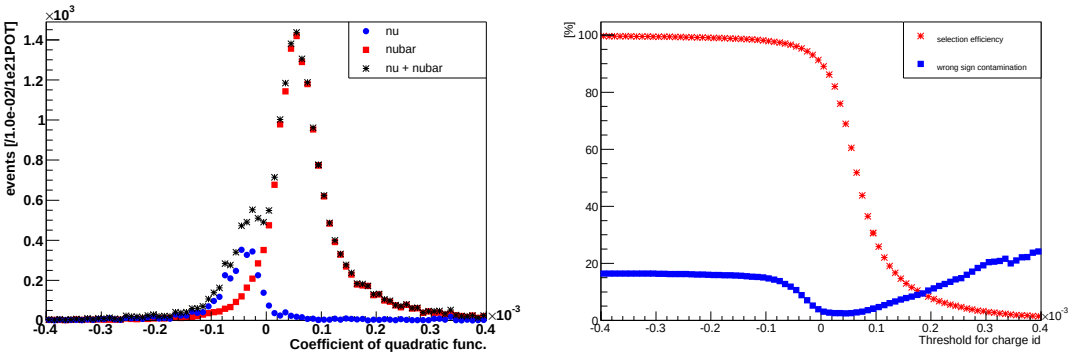

Figure 3.19: Left: Distribution of the second order coefficient of the quadratic function fitting tracks, multiplied by +1(−1) as the track is in the bottom (top) region. Right: Efficiency to correctly select $\bar{\nu}_\mu$ events and contamination of the wrong sign events (ν_μ) by the charge identification.

For different threshold values, efficiency to correctly select $\bar{\nu}_\mu$ events and contamination of the wrong sign event (ν_μ) are plotted in Fig 3.19 (right). The efficiency of $\bar{\nu}_\mu$ selection rapidly decreases around zero. The minimum value of the contamination is 2.5% at the threshold of 4.5×10^{-5}, but at that threshold value the efficiency of $\bar{\nu}_\mu$ selection already decreases down to 68.9%. On the other hand, if the threshold is set at -4.5×10^{-5} the efficiency remains 96.1% but the contamination is still 10.6%.

As a moderate solution, the threshold is determined to be zero in this study. For charge identification with threshold value of zero, the efficiency of correct identification and the wrong sign contamination after the charge identification are plotted as a function of muon kinetic energy as shown in Fig 3.20 and 3.21, respectively. The values are summarized in Table 3.8. There are two sources of the degradation of performance for reduction of wrong sign contamination.

1. Small energy events less than 200 MeV have large misidentification of charge.

This is because tracks with a few hits in the downstream MRD for small energy events might not be correctly fitted with a quadratic function.

2. Efficiency to correctly identify charge for ν_μ events is worse than that of $\bar{\nu}_\mu$. As discussed in Sec 3.6.2, some positive muons going out of the side surfaces of the MRD still remains. These unexpectedly shorter tracks to their energy might fail to be fitted correctly.

The efficiency for the low energy events, as the first issue, would be improved by combining the angular difference measurement discussed in Sec 3.5.4. This method has not been studied yet, but it will be developed with the optimization of the configuration. The second issue would not be problem with the double-slit magnetized steel plates. The magnetic field would run in one direction at the middle. Thus, the efficiency would be symmetric for $\bar{\nu}_\mu$ and ν_μ events.

Table 3.8: Efficiency of charge identification & contamination after the charge identification.

muon kinetic energy [GeV]	0 - 0.2	0.2 - 0.6	0.6 - 1.0	1.0 - 2.0
ν_μ mis-ID efficiency	42.5%	27.1%	14.2%	9.7%
$\bar{\nu}_\mu$ ID efficiency	60.3%	77.9%	90.6%	91.6%
contamination	34.6%	3.1%	1.7%	15.7%

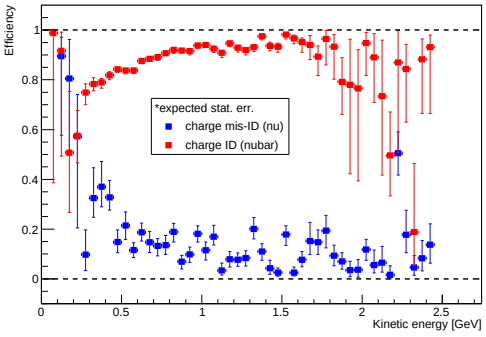

Figure 3.20: Efficiency of charge identification.

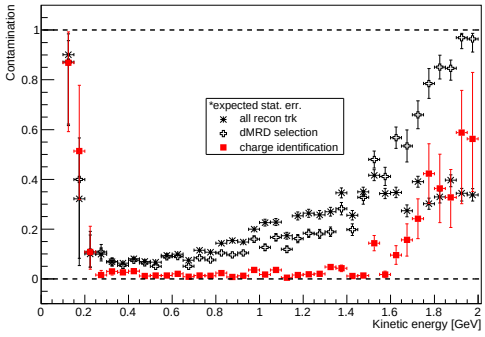

Figure 3.21: Contamination of the wrong sign neutrino events.

Table 3.9 summarizes the total number of events for each selection, the efficiencies of charge identification, and the wrong sign contaminations. The efficiency for $\bar{\nu}_\mu$ events is 89%, while that for ν_μ events is 85% (15% misidentification). The contamination of the wrong sign neutrino (ν_μ) events is decreased down to 3.2%, by a factor of five compared with the contamination for the tracks stopping in the downstream MRD.

The number of $\bar{\nu}_\mu$ events is expected to be 1.4×10^4, hence the cross section of the

charged current anti-neutrino interaction can be measured with a statistical error less than 1%.

Table 3.9: The number of events for each event selection.

	ν_μ	$\bar{\nu}_\mu$	contamination
i) All reconstruction	12446	31766	28.1%
ii) Stopping in dMRD	3287	16261	16.8%
iii) Charge identification	475	14450	3.2%
*Efficiency: iii)/ii)	14.5% (mis-ID)	88.9%	

3.7 Summary

The performance of the magnetized downstream MRD has been evaluated by the Monte Carlo simulation. Efficiency to correctly identify the $\bar{\nu}_\mu$ events by the charge of particles is expected to be 89%, and contamination of the wrong sign neutrino event ν_μ decreases down to 3% by a factor of five. The charged current neutrino interactions are extracted by reconstructing muon tracks, and the purity is expected to be 97%. Although the results do not satisfy all the requirements, it would be easily improved by the next type of magnetized steel plates with double slits, and by slight improvement of the analysis methods. The total number of $\bar{\nu}_\mu$ charged current events after the charge identification is expected to be 1.4×10^4 with 10^{21} POT. With this large statistics, it is possible to apply additional event selections when taking into account external backgrounds, and to measure further details such as deferential cross sections.

It is expected to be possible to measure anti-neutrino cross section for charged current interactions as the same accuracy level of neutrino cross section measurement.

Chapter 4

Development of firmware for NIM EASIROC module

In order to test a large number of MPPCs for WAGASCI, a NIM module with EASIROC ASIC, originally developed by Open-It project, will be used. The NIM EASIROC module contains a firmware to control the EASIROC chips. However, the former version of firmware has not included some functions required for the MPPC mass test. Hence, it is updated to satisfy requirements for the mass test. New functions requested from users are also implemented in the update.

In this chapter, the updated firmware and the results of the performance tests for the NIM EASIROC module with the updated function are described.

4.1 Requirements for the mass test of MPPC

In the performance test of 32-channel arrayed MPPCs for WAGASCI, dark noise rate, crosstalk rate, gain, and relative photon detection efficiency (PDE) will be measured with changing the temperature and bias voltage [35]. The dark noise rate is measured by counting the rate of discriminated signal with 0.5 p.e. threshold level. The crosstalk rate is measured as the ratio of the counted rate between threshold level of 0.5 p.e. and 1.5 p.e. The gain and relative PDE is measured by injecting LED light. To measure the MPPC performance, the readout electronics are required:

- to operate at least 32 channels of MPPCs at the same time,
- to provide bias voltage with around 55 V and adjust it for a range of 4 V,
- to acquire ADC value of charge from MPPCs,
- and to count the discriminated signals up to 1 M counts per second.

4.2 NIM EASIROC module

The NIM EASIROC module has been developed by KEK and Open-It as an asynchronous readout system of multi-channel MPPCs. Figure 4.1 shows the front side of the board, and Fig. 4.2 shows the conceptual diagram of the board. The NIM EASIROC module controls up to 64 MPPCs by two EASIROC chips. It provides bias voltage for the MPPCs with its adjustments by EASIROC. The bias voltage is monitored by a monitor ADC. Analog signals from the EASIROCs are converted by four ADCs and transferred as digital signals to an FPGA. Data transfer between the FPGA and a data acquisition (DAQ) PC is done through Ethernet. Power for the whole module is taken from the back-panel by either +6 V AC power supply or NIM power supply.

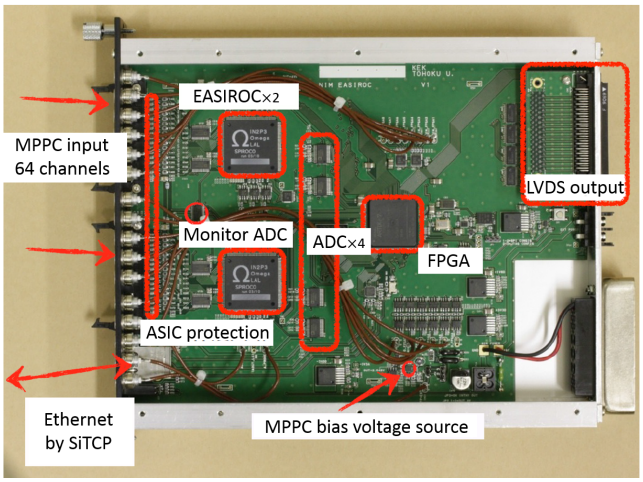

Figure 4.1: The front side of the NIM-EASIROC board. [36]

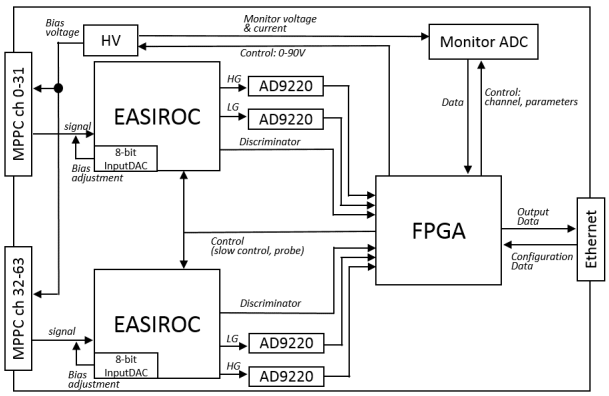

Figure 4.2: The conceptual diagram of the NIM-EASIROC board.

4.2.1 EASIROC chip

Figure 4.3 shows the block diagram of EASIROC. Each function of EASIROC is briefly explained as follows.

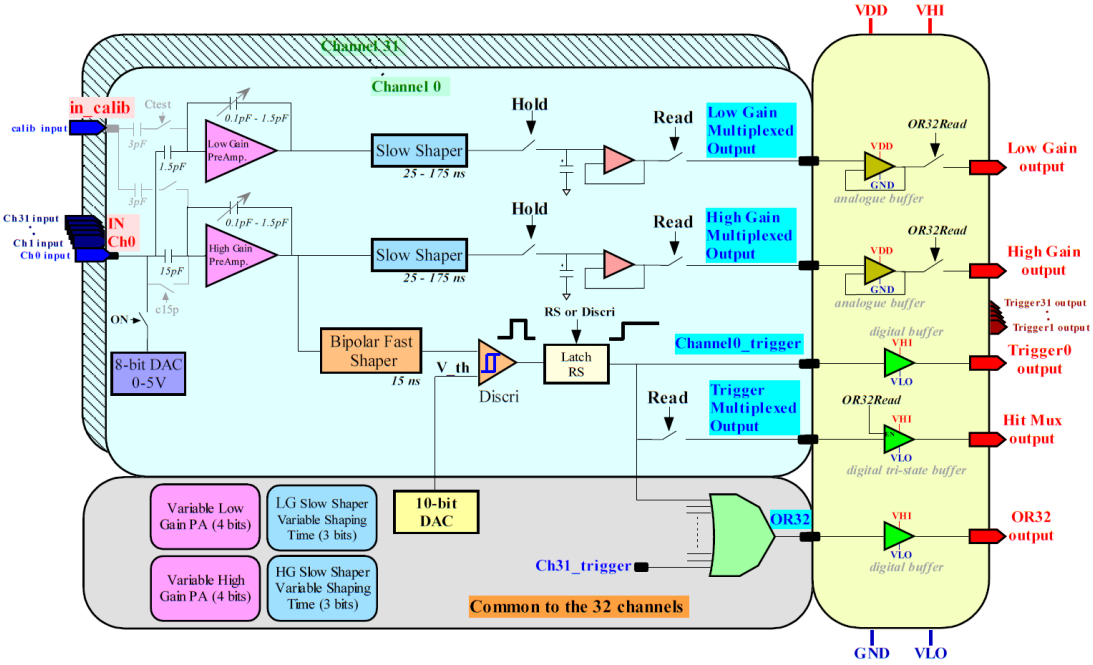

Figure 4.3: The block diagram for the EASIROC chip. [37]

Preamp

The chip contains two preamps with different gains for each channel. They are only active to positive charge from MPPCs with AC coupled. The high gain preamp amplifies the signal by gain of 10 to 150 and the low gain one does by gain of 1 to 15. Two different gains allow the chip to obtain a wide dynamic range for the input charge, from 160 fC to 320 pC. This range corresponds to the photo electrons of 1 p.e. to 2000 p.e., assuming that the MPPC's gain is 10^6.

8-bit Input DAC

Each of the charge input line is equipped with 8-bit DAC to adjust the ground level of the MPPC anode. It works as the adjustment of the bias voltage for each channel by decreasing the value up to 4.5 V.

Fast shaper & Discriminator

A signal after the high gain preamp is shaped by a fast shaper with shaping time of 15 ns. A discriminator after the fast shaper determines if the signal is over a threshold common for all channels. The discriminated signals of 32 channels are output from the chip in parallel. An OR signal of the 32-channel discriminator signals is also output. A function to take a latch of the discriminator signal exists, but is not used in the test measurement of WAGASCI.

Slow shaper

Signals from the preamps with high gain and low gain are shaped by slow shapers. The shaping time can be varied from 25 ns to 175 ns every 25 ns. "Track & Hold" circuits after the slow shapers receive a HOLD signal to memorize the voltage of the slow shaper signals at that time with capacitors. The analog values memorized on the capacitor for all channels are output serially for each of high gain and low gain.

"Slow control" register

Configuration of the chip is done with slow control registers. It controls the chip parameters, such as the feedback capacitor for the preamp, 8-bit Input DAC, 10-bit threshold DAC, and shaping time of the slow shaper. The configuration data needs to be sent serially to the chip with a control clock signal and a load signal. Lines of the configuration data are shared between the slow control registers and probe registers, and switched by a digital input to the chip.

"Probe" register

Configuration with the probe registers enables to select an analog signal from the high/low gain preamp, slow shaper with high/low gain preamp, and fast shaper. The selected signal is probed out of the chip.

"Read" register

The analog memories in the chip for high gain and low gain are probed out of the chip, and controlled by the read registers. A channel to be probed out needs to be selected by the registers, and otherwise the these outputs are fixed at high impedance.

Calibration charge input

Instead of using the charge input from MPPCs, the chip is also able to inject the calibration charge provided inside the chip. When the 3 pF calibration capacitor is enabled by the slow control, the connection to the signal input is shut down and both preamps of high gain and low gain are connected to the calibration capacitor.

4.2.2 ADC

The analog outputs from the slow shapers in the EASIROC chip are converted by four 12-bit pipeline ADCs (AD9220 [38]). Each analog signal with high/low gain from the two chips is converted in parallel and transfered to the FPGA.

4.2.3 FPGA

The digital signal processing on the NIM-EASIROC board is done by Field Programmable Gate Array (FPGA). An Artix 7 series FPGA (XC7A100T-2FGG676C [39]), product by Xilinx, is used. Table 4.1 shows the main device resources of the Artix 7 series. It is composed of a large number of configurable logic blocks (CLB) [40], which contains two logic cells (SLICE). Each SLICE contains four SRAMs (Look Up Table, LUT) with random logic implementation, and eight flip-flops as well as multiplexers and arithmetic carry logic. 30% of the SLICEs are able to be used as distributed memories (Memory LUTs). Artix 7 series also includes dual-port 36 Kbits Block RAMs, enabling to store data independently of CLBs.

Another feature of Artix 7 series is clock management. It has six clock management tiles (CMTs), which serve as frequency synchronizers and as jitter filters, as well as phase shifters. It allows clock distribution with different frequencies and phases in the FPGA with an external clock source.

Configuration of the firmware mainly means providing information on LUTs, as well as alignment of the connections between CLBs.

Table 4.1: The device resources of XC7A100T-2FGG676C

Name	Number
SLICE	15850
Logic LUTs	63400
Maximum Memory LUTs	19000
I/O	300
Block RAM Tile	135
CMT	6

4.2.4 Monitor ADC

In order to monitor the values of bias voltage, bias current, bias voltage adjustments for each channel, and temperature, an ADC (AD7795, ANALOG DEVICES [41]) is mounted on the board. One thirtieth of the bias voltage from the bias voltage source is provided into the monitor ADC. 20% of the bias current is also provided and measured as voltage. Each value of 64 8-bit Input DACs is measured through four 16-channel multiplexers (ADG706 [42]). The input for temperature is not used so far.

Configuration of the monitor ADC is done with the communication registers. The output of the monitor ADC is sent as a serial signal to the FPGA.

4.2.5 Bias voltage source

In order to supply bias voltage for MPPCs, a 90 V Boost DC/DC Converter (LT3482, Linear Technology [43]) is mounted on the board. The bias voltage source uses output of a 16-bit digital-to-analog converter (DAC8411, TEXAS INSTRUMENTS [44]) as a reference voltage. It controls bias voltage supply for MPPCs from 0 to 90 V.

4.2.6 Interface

On the front-panel of the module are NIM inputs/outputs, including 6 digital signal inputs, 5 digital outputs, and 5 analog outputs. The digital inputs and outputs are connected to the FPGA and configurable. The analog outputs are used for the analog probe and high gain output from the two EASIROCs, and output of the bias voltage source. There are also two 32-channel inputs for MPPCs with 68-pin connectors for its cathode and anode, including two temperature lines. An Ethernet connection is put for TCP/IP and UDP, too.

4.2.7 Other components

SPI flash memory

The SRAM-based configuration of FPGA is volatile, thus an SPI flash memory (M25P32, Micron [45]) contains configuration data of the FPGA and reconfigures it every reboot.

Front-panel LEDs

Four LEDs (Dialight 568-0721-111 [46]) are on the front-panel of the module, and their behavior with red and green light is configurable. They are currently configured as follows.

- LED1 turns on while the NIM module is powered on. Green means the TCP connection running and red means its not running.
- LED2 turns on red while there is a busy signal in the firmware.
- LED3 becomes green as OR signal of all 64 discriminators comes.
- LED4 becomes green with the MPPC bias voltage over 5 V.

50 MHz clock oscillator

An 50 MHz clock source (KC7050B50.0000C31A00, KYOCERA [47]) provides the reference clock signal to the FPGA.

4.3 Development of new firmware

Table 4.2 shows functions of the former version of firmware for the NIM EASIROC module, and the firmware for another utilization of EASIROC with a VME module [48]. The former firmware for the NIM EASIROC module contains ADC control, data transfer by SiTCP [49] [50], EASIROC slow control, bias voltage source control, and monitor ADC control. However, it does not include a scaler function, which is required in the MPPC mass test. A TDC function is not implemented either, although it has been required by users for further utilization of EASIROC. On the other hand, the VME version of firmware has the basic functions required in the new firmware implemented.

Table 4.2: The firmware functions.

	Former ver. for NIM module	Another utilization (VME ver.)
ADC control	◯	◯
TDC	×	◯
Scaler	×	◯
SiTCP data transfer	◯	◯
EASIROC slow control	◯	◯
Bias voltage source control	◯	×
Monitor ADC control	◯	×

To implement the scaler and TDC, the VME version of firmware is inherited into the new firmware first. It is modified to match the pin alignment on the NIM EASIROC module. Second, unique functions for the NIM EASIROC module, such as control of the bias voltage source and monitor ADC, are newly implemented to match the new firmware. Furthermore, other new functions, such as selectable logic, signal width adjuster, calibration charge injection, and clock signal output, are also implemented with this development.

4.3.1 Development procedure

The firmware development is done with Vivado Design Suite (version 2014.3.1) [51], which is a tool suite for designing, integrating, and implementing the firmware with Xilinx 7 series FPGA. It allows an automatic management of the register transfer level (RTL) source written by hardware description language (HDL) and constraints. Logical simulation is also done for each firmware module in RTL design. The RTL design is synthesized into gate level representation, and furthermore transformed into physical array of the target FPGA device by logic optimization, placement of logic cells, and routing of connections between cells. The developed circuit information is implemented into the FPGA as a bitstream file through JTAG connection.

A block diagram of the new firmware is shown in Fig 4.4. It contains the EASIROC data acquisition with ADC, multi-hit TDC (MHTDC), and scaler through SiTCP.

Each trigger signal is controlled by the trigger manager. The clock manager distributes clock signals from the external 50 MHz clock source. The other components, such as the EASIROC configuration, control of the monitor ADC and bias voltage, and newly added functions, are controlled through the remote bus control protocol (RBCP) bus.

Timing delay of data and clock signals between flip-flops in the new firmware are calculated with Vivado, and it is checked if the timing satisfies the requirements for correct data capture (See more detail in Appendix C). It is confirmed that all the data and clock signals are operated within expected timing.

Table 4.3 summarizes usage of the FPGA device with the new firmware. The number of occupied LUTs is 17996, that is 28.4% of the total LUTs. The device is not fully occupied yet. Table 4.4 is occupation of the main components in the firmware. The most dominant component is the MHTDC module and occupies 53.9% of the whole firmware.

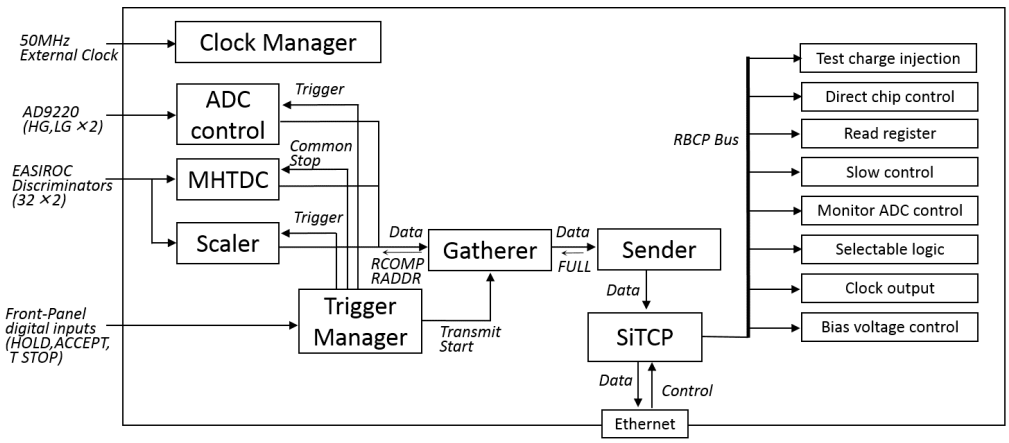

Figure 4.4: The block diagram for the firmware.

Table 4.3: Usage of the FPGA device.

Name	Utilization
Logic LUTs	17996 (28%)
Memory LUTs	4656 (25%)
I/O	213 (71%)
Block RAM Tile	29 (21%)
CMT	2 (33%)

Table 4.4: Occupation of the main components.

Name	Occupation
MHTDC	54%
SiTCP	20%
Signal width adjuster	14%
Scaler	4%
ADC	3%
Gatherer	1%
The others	4%

4.3.2 Inherited functions from the VME version of firmware

ADC control

The ADC control module receives data from the four ADCs, and transfers the data to the gatherer module through double buffers. Four core modules work at the same time for each ADC. This module also sends 3 MHz clock signals to the EASIROC chips and ADCs for data readout. Dead time of this module is about 12 μs, including readout of 32 channels and conversion at the ADCs.

MHTDC

The MHTDC module measures the timing of the 64-channel discriminator signals at their leading edge and trailing edge with 1 ns resolution. The high resolution is achieved by using four 250 MHz clocks with different phases. Data transfer is done with 125 MHz. 16-deep ring buffers are used in this module, and store timing information of the latest 16 hits. The timing information is measured as time difference from the discriminator signal to a common stop signal. Time window is controlled with the range of 0 to 4095 ns.

Scaler

The scaler module counts the number of the discriminator signals for each channel and their OR signals. This module contains 69 12-bit counters, including two clock counters with 1 kHz and 1 MHz, 64 for each channel, and three for the OR signals with 32 channels for each chip and all the 64 channels. All the counters are reset at the same time as the common stop. Data for each counter are gathered with information of channel number and overflow, and transferred through double buffers.

Gatherer and sender

The gatherer module and the sender module transfer data from ADC control, MHTDC, and scaler to the SiTCP module. The gatherer module starts data transfer after receiving a transmit start signal. It gathers data from double buffers in each module, counts the number of words, and combines the data with a header tag. The sender module receives the data with header. It converts the number of words from 32 bits to 8 bits in order to match SiTCP and sends it to the SiTCP module serially by 8 bits.

Trigger manager

The trigger manager module receives three front-panel digital inputs, named HOLD, T STOP, and ACCEPT, in this order. It synchronizes the inputs with the internal clock, and sends the following trigger signals: i) a trigger signal to the ADC control module and a hold signal to the EASIROC chips, ii) a common stop signal to the MHTDC module and scaler module, iii) and a transmit start signal to the gatherer module. The hold signal is extended for 2 μs. A busy signal is also managed by this module.

Table 4.5: Clock signals by the clock manger module.

Frequency	Usage
3 MHz	Controlling the ADCs
6 MHz	Slow control and ADC control
25 MHz	SiTCP
66 MHz	Controlling SPI FLASH memory
125 MHz	MHTDC and scaler
250 MHz	TDC sampling with different phases of 0°, 90°, 180°, and 270°
500 MHz	Trigger manager

Clock manager

The clock manager module distributes internal clock signals with different frequencies and phases from the external 50 MHz clock. All the clock signals are produced with two of the CMTs as shown in Table 4.5.

SiTCP

The SiTCP module transfers data between the Ethernet connection and the firmware. The data transfer to the DAQ PC from the firmware is done with TCP/IP, and it works in the same way as an 8-bit synchronized FIFO. In addition, the user control of the firmware from the PC is done by RBCP bus. The data bus is with 8 bits and the address bus is with 32 bits, and it allows many modules to be connected on this bus through UDP. The SiTCP library is distributed by Bee Beans Technologies [52].

Slow control

The slow control module receives the EASIROC configuration data from the SiTCP module, and sends the corresponding bit stream with 456 bits to the chip. The transfer starts as a cycle start signal arrives from the direct chip control module.

Direct chip control

The direct chip control module controls reset, validation, and load signals for the EASIROC chips. Selection between the slow control and probe register is also done with this module.

Read register

The read register module controls 160-bit configuration data and clock signals of the EASIROC read register.

Status register

The status register module arbitrarily selects the DAQ modes from ADC, MHTDC, and scaler.

4.3.3 Unique functions to the NIM EASIROC module

Bias voltage source control

Figure 4.5 shows the block diagram of the bias voltage source control module. Value of the bias voltage is controlled with 16 bits, combining the higher 8 bits and the lower 8 bits. The 16-bit data in this module is serially sent to the 16-bit DAC through a register shifter. The serial data transfer starts after a start signal is sent. To control the 16-bit DAC, a 25 MHz clock signal is used. The 90 V DC/DC converter is enabled as the NIM module is powered on, but can be turned off by user control.

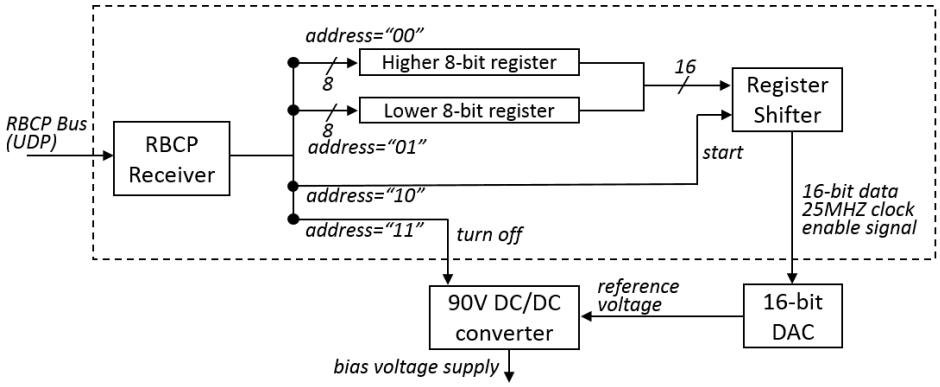

Figure 4.5: The block diagram for the bias voltage source control module.

Monitor ADC control

Figure 4.6 shows the block diagram of the monitor ADC control module. It includes a core module, which decodes serial output from the monitor ADC into 16-bit data and transfers it to the SiTCP module by 8 bits. The core module also interprets configuration data of the monitor ADC. The configuration includes selection of a readout channel, gain value, ADC input range, single/continuous readout, single/continuous conversion, operation frequency, and so on.

4.3.4 Other new functions

Signal width adjuster

Figure 4.7 shows the block diagram of the signal width adjuster module. This module is required to adjust widths of discriminator signals from EASIROC. For taking com-

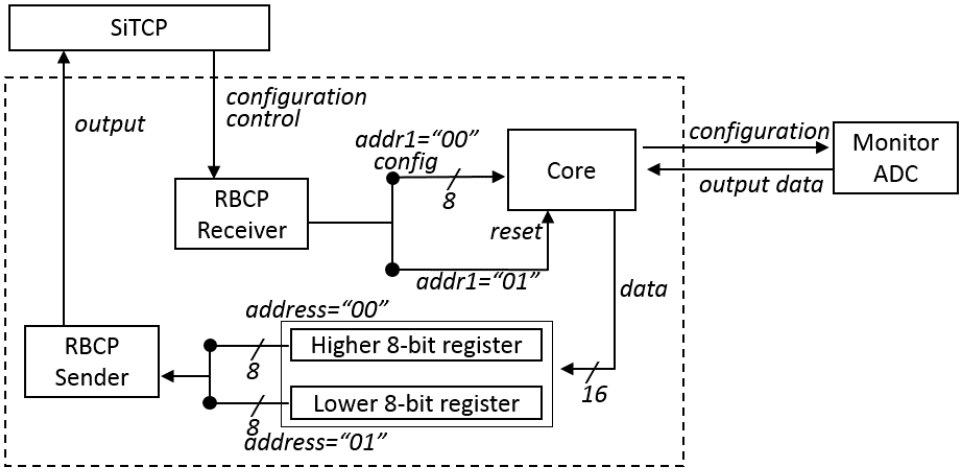

Figure 4.6: The block diagram for the monitor ADC control module.

bination logic of them, adjustable widths are useful.

It contains 64 width adjusters for each discriminator signal as shown in Fig 4.8. An input signal is cut at a next edge of 125 MHz clock by a sharpener shown in Fig 4.9 . The sharpened input signal is also delayed by a delayer shown in Fig 4.10. A leading edge of an output signal is set at the leading edge of the sharpened input signal, and a trailing edge of the output signal is set at the delayed signal. The length of this delay is adjusted from 40 ns up to 800 ns by 8 ns step.

The leading edge of the width-adjusted signal is synchronized with the raw discriminator signal from EASIROC. The trailing edge is not synchronized with the raw discriminator signal, but synchronized with 125 MHz clock signal in the firmware. This adjusted trigger is probed out to the front-panel TRIG output through the selectable logic module.

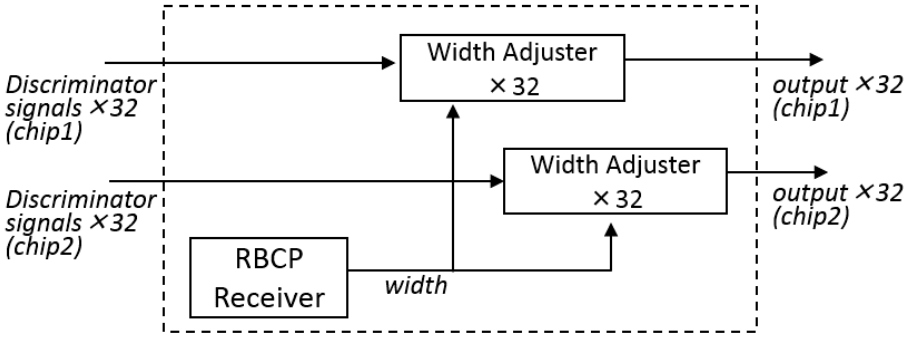

Figure 4.7: The block diagram for the signal width adjuster module.

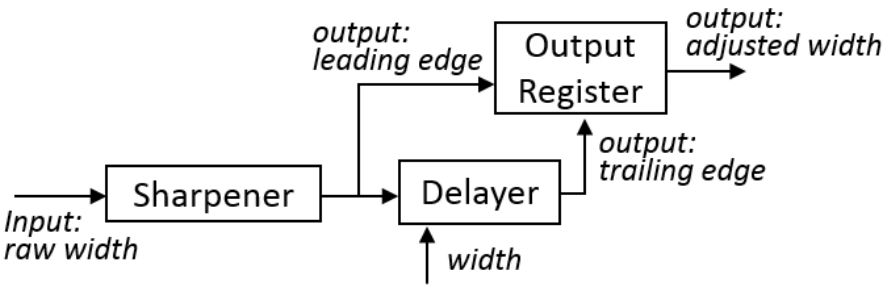

Figure 4.8: The block diagram for the width adjuster module for each signal.

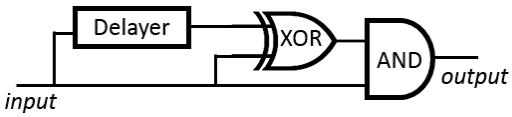

Figure 4.9: The block diagram for the sharpener module.

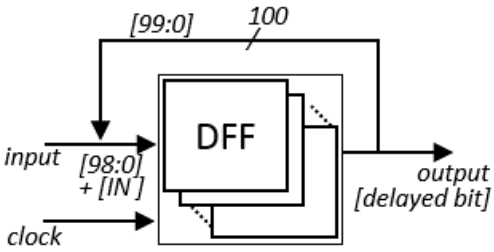

Figure 4.10: The block diagram for the delayer module.

Selectable logic

Figure 4.11 shows the block diagram of the selectable logic module. Using the width-adjusted discriminator signals, combination logic of the signals are controlled and probed out from the front-panel TRIG output. A logic pattern is selected from:

- Single channel,
- OR signal of a chip,
- OR signal of all 64 channels,
- ⟨OR signal of chip 1⟩ AND ⟨OR signal of chip 2⟩,
- ⟨OR of channel 0 to 15⟩ AND ⟨OR of channel 16 to 31⟩
  AND ⟨OR of channel 32 to 47⟩ AND ⟨OR of channel 48 to 63⟩,
- AND logic of selected channels in a chip or all 64 channels,
- ⟨AND logic in chip 1⟩ OR ⟨AND logic in chip 2⟩.

A threshold for the number of hits is optionally set. Each OR signal is active only when the number of present discriminator signals is equal to or more than the threshold.

The threshold does not affect AND logic. Channels used for the AND logic are also selectable.

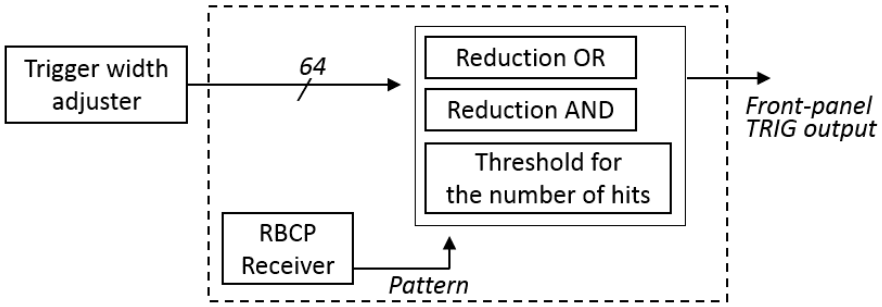

Figure 4.11: The block diagram for the selectable logic module.

Calibration charge injection

Figure 4.12 shows the block diagram of the calibration charge injection module. This module enables the calibration charge injection inside EASIROC. The module is operated by the 125 MHz clock and reset by an external supervisory circuit (TPS3103K33DBVR, TEXAS INSTRUMENTS [53]). It provides a signal for calibration input of the EASIROC chip for 8 ns every 130 ms.

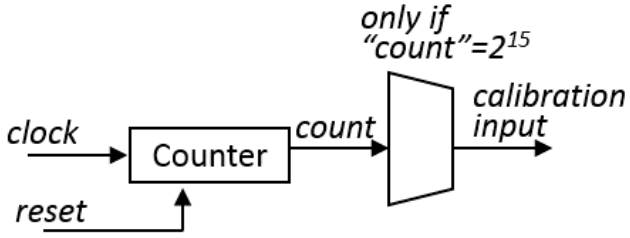

Figure 4.12: The block diagram for the calibration charge injection module.

Clock signal output

Figure 4.13 shows the block diagram of the clock signal output module. The input 3 MHz clock signal, which is produced by the clock manager module, is counted up and controls the output signal. Two parameters, corresponding to the output clock period and the half-period, control the counts to determine each of a rising edge and a falling edge of the output signal. The output signal is probed out from the front-panel NIM output. The output signal is selected from:

- OFF (low level, by default),
- ON (high level),
- and clock signals, with frequency of 1 Hz, 10 Hz, 100 Hz, 1 kHz, 10 kHz, 100 kHz, 3 MHz.

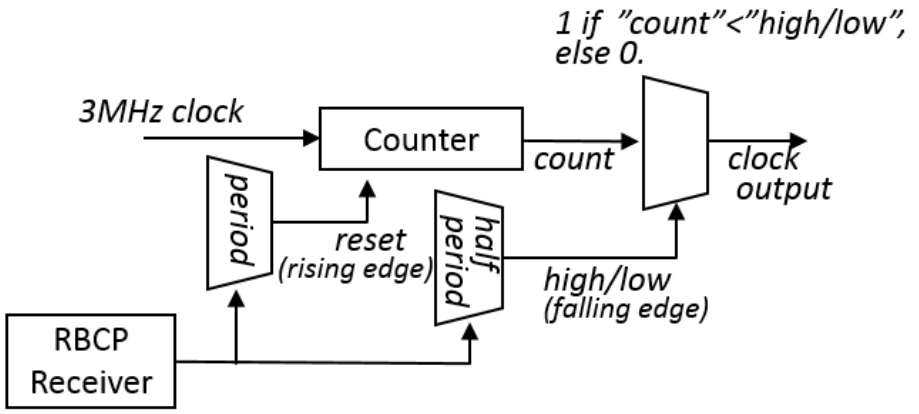

Figure 4.13: The block diagram for the clock signal output module.

4.4 Performance test of the NIM EASIROC module with the new firmware

4.4.1 Operation of slow control, probe register, and read register

The modules of slow control, probe register, and read register were already implemented into the VME version of firmware, and already confirmed to correctly control EASIROC. However, their behavior is checked in order to confirm the new firmware operation on the NIM EASIROC module.

As injecting test charge into MPPC input of the NIM EASIROC module, an analog signal inside the EASIROC chip is monitored by an oscilloscope.

Hold signal timing and width

Slow shaper signals inside the EASIROC chip are probed out of the front-panel output for a channel selected by the read register. A hold signal is produced by the trigger manager module in the firmware in accordance with the front-panel HOLD input. It holds analog value of the slow shaper signals at the corresponding timing.

Figures 4.14 and 4.15 show the slow shaper signals with different timings of HOLD inputs. It is confirmed that the hold signal produced in the firmware is correctly sent to the chips with the timing of the front-panel HOLD input. The hold signal produced by the trigger manager module is extended for 2 μs as designed as shown in Fig 4.16.

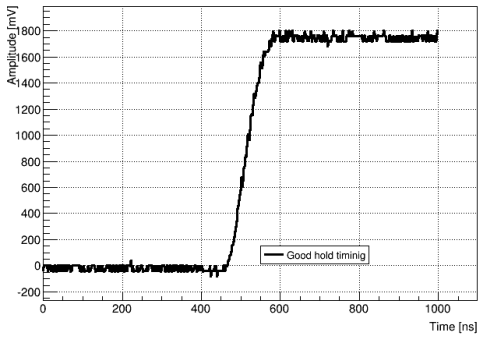

Figure 4.14: The slow shaper signal with good timing HOLD input.

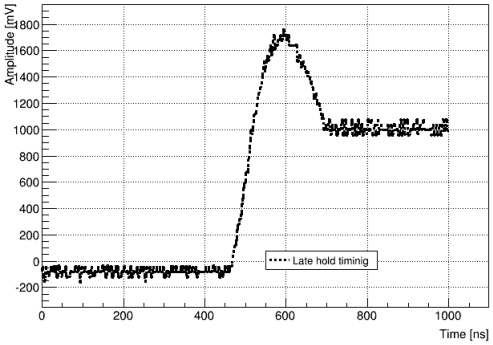

Figure 4.15: The slow shaper signal with late timing HOLD input.

Feedback capacitor of block controlled by slow control

Preamp signals inside the EASIROC chips are probed out of the front-panel output for a channel selected by the probe register. The probed waveform of preamp signals is not the whole waveform after the preamp, but just around the peak. Gain value with high/low gain is controlled as changing value of the feedback capacitor of the preamps by the slow control.

Figure 4.17 shows the probed preamp signals, as changing the feedback capacity. It is confirmed that the gain is correctly controlled by the slow control. The gain value increases as the feedback capacitor value decreases as expected.

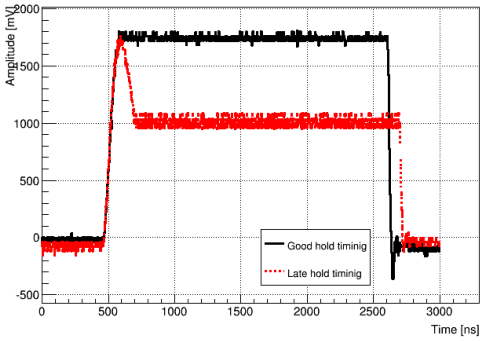

Figure 4.16: The slow shaper signal with the 2 μs hold signal.

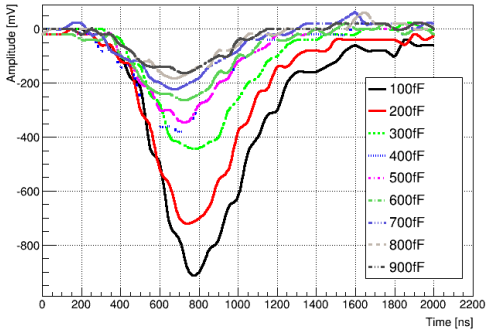

Figure 4.17: Preamp signals with different feedback capacitor values.

4.4.2 Calibration and operation check of the bias voltage control and monitor ADC

The former firmware for the NIM EASIROC module has already controlled the bias voltage source and monitor ADD. However, operation checks of these modules updated

to the new firmware are required, as well as their calibration for the usage between voltage and DAC value.

Output of the bias voltage source is optionally probed out to the front-panel NIM output by a jumper pin on the board. The probed voltage is measure by multimeter (PC20 [54]) with 1% accuracy in accordance with 16-bit DAC input. Voltage of the 8-bit InputDAC values are also controlled and measured as the voltage level of the corresponding MPPC signal line. These values are monitored by the monitor ADC, and the output values are checked as controlling the bias voltage and the 8-bit InputDAC.

Figure 4.18 shows the relation between the probed out bias voltage and the 16-bit DAC input. The bias voltage is controlled as expected as it increases in proportion to the 16-bit DAC value up to 92 V. At the same time, the outputs of the monitor ADC for the bias voltage and current behave in the same way as the bias voltage supply. The output value of the monitor ADC is always observed to be stable within ±2 digits, except for measuring small value less than 1 V. The monitor ADC value for the 8-bit InputDAC is also confirmed to be consistent with the voltage measured at the MPPC signal lines.

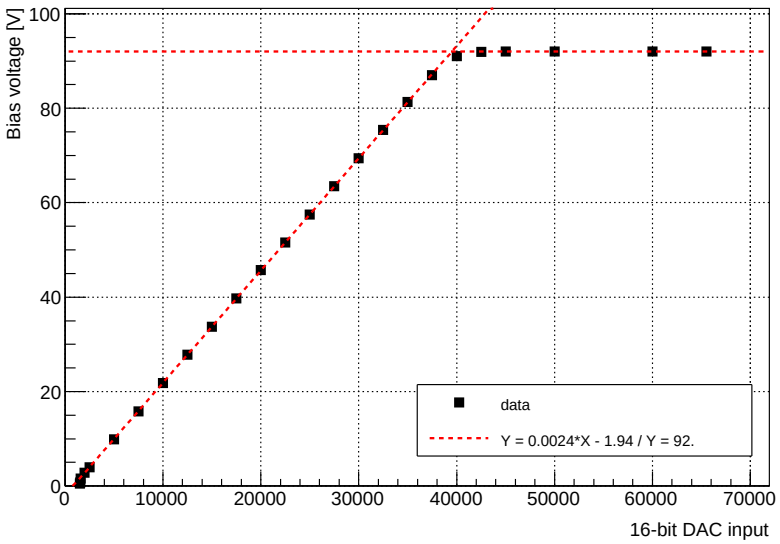

Figure 4.18: Plots: Bias voltage supply to the input 16-bit DAC value. Dotted lines: Linear lines ($y = 2.4 \times 10^{-3}x - 1.94$ and $y = 92.0$)

4.4.3 Operation test of the new functions

The newly implemented functions, such as signal width adjuster, selectable logic, clock signal output, and calibration charge injection, are required to be tested if the functions could be operated as expected.

Signal width adjuster

As probing out the width-adjusted discriminator signal, the width is varied and is measured with an oscilloscope.

It is confirmed that the average value of the signal width is controlled linearly as designed. Figure 4.19 shows the discriminator signal with raw width and with adjusted width of 680 ns, together with a synchronized signal to the charge injection. It shows that the leading edge of the width-adjusted signal is synchronized with the leading edge of the raw signal, and the trailing edge is deviated from the average by ± 4 ns as designed.

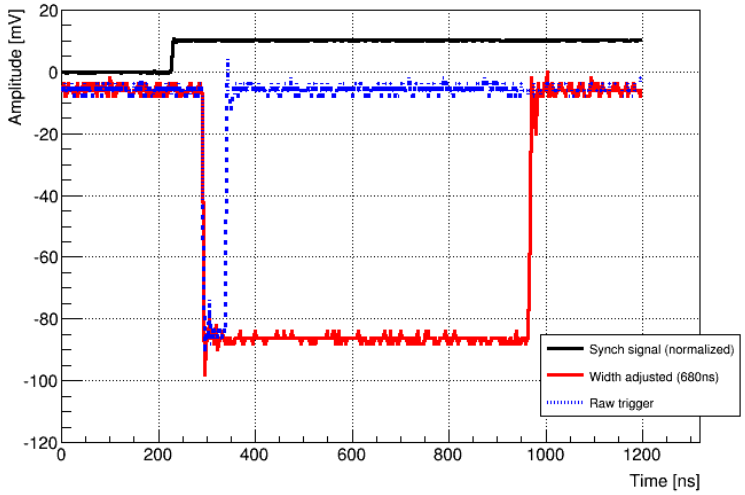

Figure 4.19: The raw trigger signal and the trigger signal with the adjusted width.

Selectable Logic

Test pulses are injected to up to four channels of the MPPC inputs at the same time, and the front-panel TRIG output is checked. Although the number of the tested patterns is limited because of only four inputs at the maximum, it is so far confirmed that the logic pattern is controlled as designed, for combination of OR and AND logic and threshold for the number of hits.

Clock signal output

The clock signal is probed out from the front-panel NIM output, and its frequency is controlled. Figures 4.20 and 4.21 show the 100 kHz clock signal and 3 MHz clock signal respectively. The frequency is measured by the oscilloscope and the difference from the input frequency is less than 0.01%. Although small spikes at the edge are observed with the 3 MHz clock signal, all the waveform of the clock signal is observed as rectangular waves as designed.

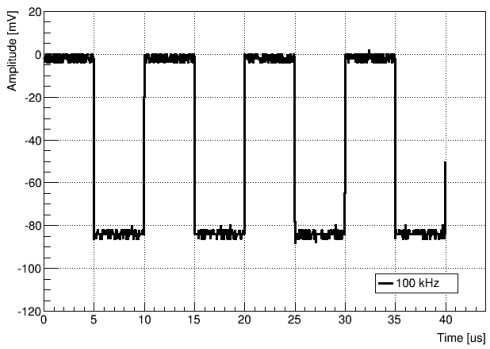

Figure 4.20: 100 kHz clock signal output.

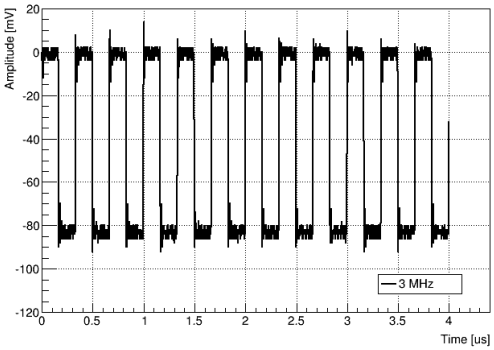

Figure 4.21: 3 MHz clock signal output.

Calibration charge injection

As enabling the calibration charge injection by the slow control, the ADC distribution is checked. Figure 4.22 shows the ADC distribution with the calibration charge injection when the 8-bit Input DAC is ON with a value of 400. A single sharp peak is observed, and it means that the constant calibration charge is produced inside the chip as designed. With the Input DAC OFF with a value of 100, however, the ADC distribution is deviated as shown in Fig 4.23. This deviation is a known feature of EASIROC. The operation with Input DAC OFF should be avoided because the signal becomes unstable.

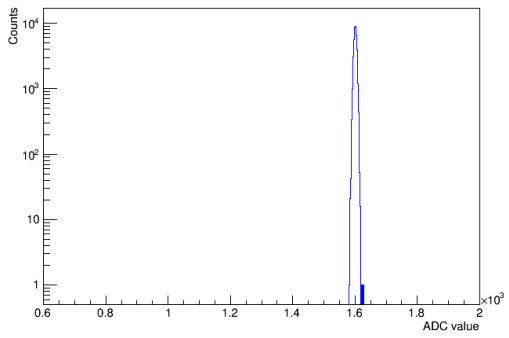

Figure 4.22: Calibration charge with the InputDAC of 400 (ON).

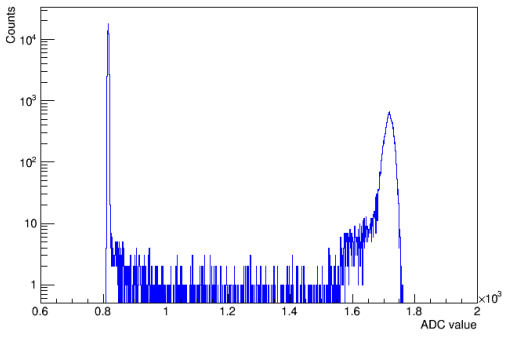

Figure 4.23: Calibration charge with the InputDAC of 100 (OFF).

4.4.4 The module performance test by the injection of test pulse

After it is confirmed that each component of the firmware correctly behaves and succeeds in the communication with the EASIROC chips, the performance as the NIM-EASIROC module with the new firmware, such as ADC response to input charge, time resolution of MHTDC, scaler's behavior, and multi-hit separation, is measured by

injecting test charge into the MPPC input pins. The used modules are listed in Table 4.6.

Table 4.6: The modules for the measurement with test pulse injection.

Module	Type
80 MHz Function Generator	Agilent 33250A [55]
8ch Gate & Delay	Technoland Corporation N-TM 205 [56]
TTL-NIM Level Converter	HOSHIN N002 [57]
4input-4ch FAN IN/OUT	HOSHIN N007 [58]
Attenuator	KEK8607 N0411-0596

ADC response to input charge

The basic setup of the ADC measurement is shown in Fig 4.24. Injecting a pulse with constant voltage to a capacitor, the corresponding constant charge is provided into the EASIROC chips. There are one positive charge at the rising edge of the voltage input pulse and one negative charge at the falling edge. Hence the pulse width is taken as $1\,\mu$s, that is long enough for the negative charge not to cancel the leading positive charge.

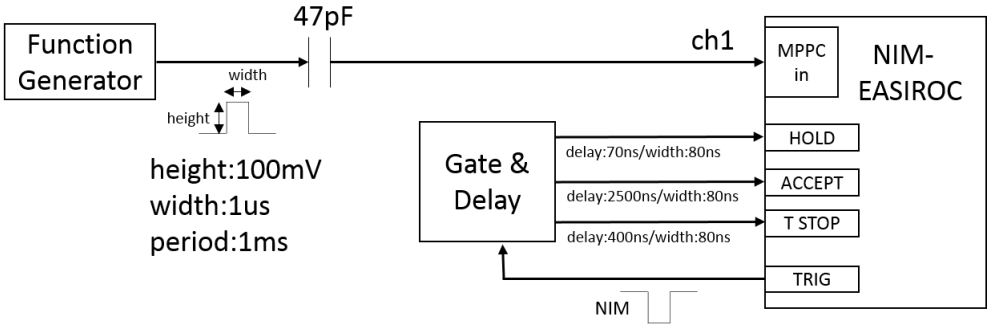

Figure 4.24: The setup for measurements of ADC response to the test charge injection.

The response of the ADC is measured with changing the amplitude of injection pulse, with the feedback capacitors of 200 fF for both of high and low gains. Each distribution of ADC values is fitted with a Gaussian function. The mean value of the Gaussian is regarded as the average ADC value for the injection charge. Taking ten thousands events for each measurement, its statistical errors are 1%. The Gaussian sigma includes accuracy of the ADC measurement of the NIM EASIROC module and fluctuation of the injected charge, but it is so small as to less than 1%. The average ADC values are plotted as functions of injected charge from the capacitor as shown in Fig 4.25. As expected, it is confirmed that the values with high gain behaves in linear

for small input charges up to a few pC, and the values with low gain does for large input charge around a few dozens pC.

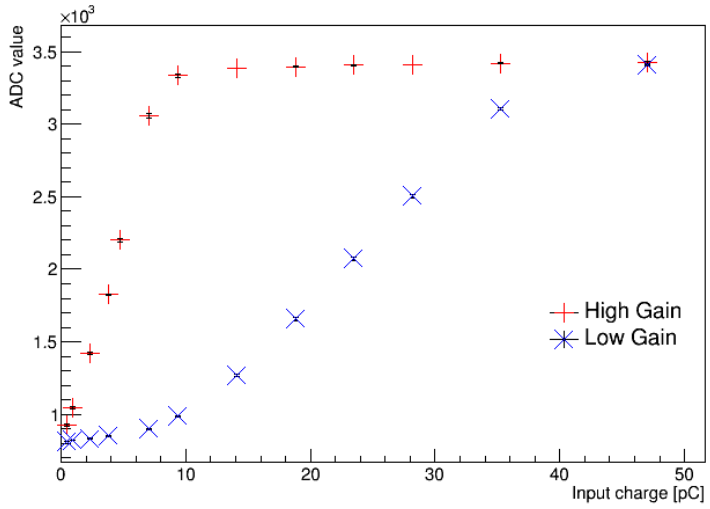

Figure 4.25: The output ADC values to the charge injection.

Time resolution of MHTDC

For the time resolution measurements, the setup as shown in Fig 4.26 is used. Test charge is injected, and trigger signals are synchronized with the charge injection through the synchronous signal of the function generator.

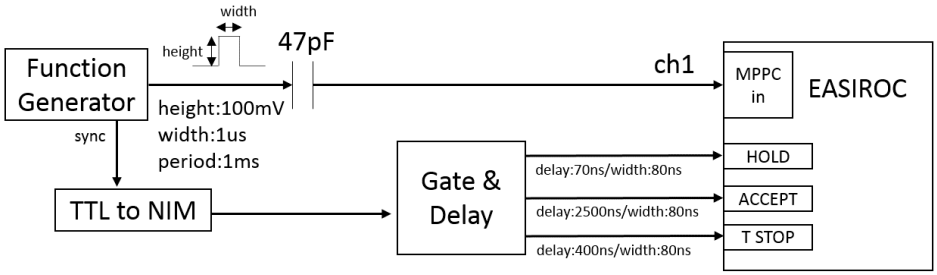

Figure 4.26: The setup for the time resolution measurements.

Figure 4.27 shows the TDC distribution for about 55 million events and a Gaussian fitting the TDC distribution. The time deviation includes:

- precision of discriminator signal timing in the EASIROC chip,
- precision of delayed signal for the common stop signal by the Gate & Delay NIM module,

- accuracy of the MHTDC module in the firmware,

- and fluctuation of arrival timing of signals in the EASIROC module.

The precision of the function generator does not need to be considered because the TRIG front-panel output is synchronized with the discriminator signal. The fluctuation of the Gate & Delay signals is negligibly small, thus the whole deviation is the time resolution of the NIM-EASIROC moduel. As 1σ of the Gaussian function, the time resolution is measured to be 0.53 ns.

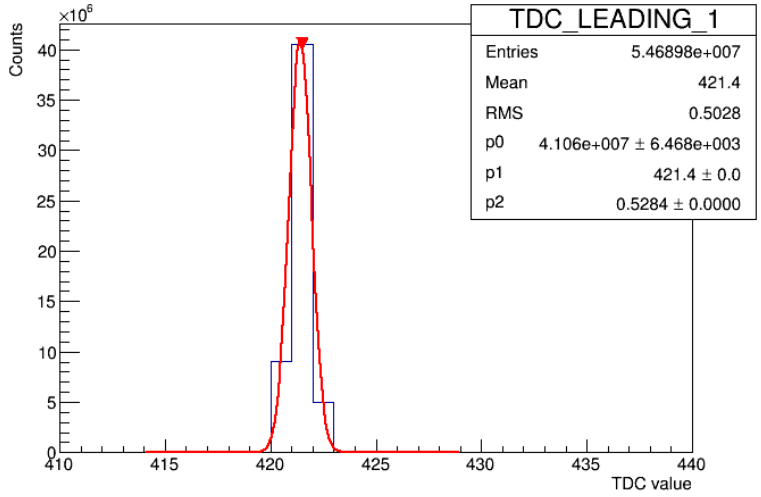

Figure 4.27: Histogram: Distribution of MHTDC value with test pulse. Fitting line: Gaussian fitting of the histogram.

Scaler's behavior

The scaler measurement uses the setup shown in Fig 4.28. The front-panel clock signal with 1 kHz is used as input to the Gate & Delay module for triggers, thus the triggers are asynchronous with the function generator signals. The function generator signals are sent from the front-panel digital input to the internal FPGA, and their frequency is varied. The front-panel input is connected to input of the scaler module in the firmware, only for this test measurement.

Figure 4.29 shows the number of counts per 1 ms as a function of the frequency of the input pulse, and Fig 4.30 shows the ratio. Scaler counts are consistent with the frequency of the input pulse by the accuracy of 0.5% up to 100 kHz, and 2% up to 2 MHz.

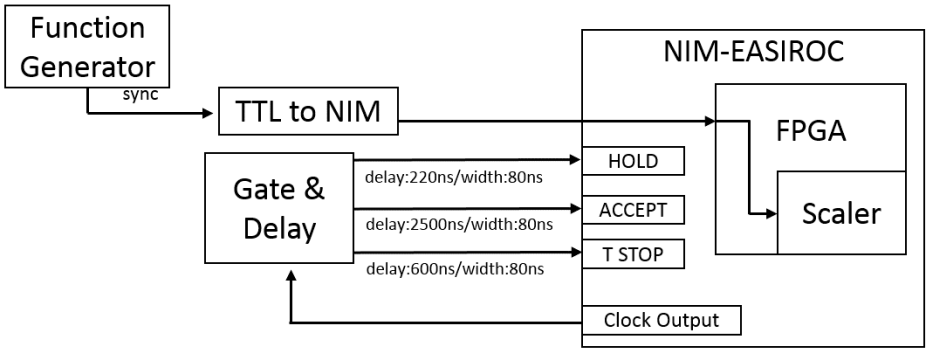

Figure 4.28: The setup for the scaler measurements.

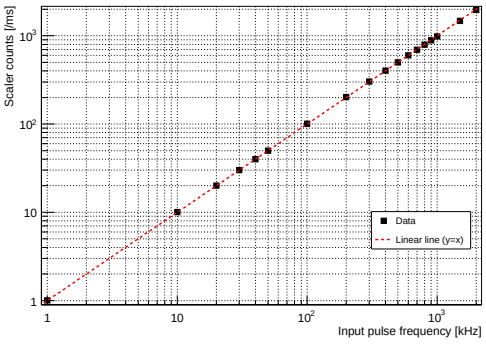

Figure 4.29: Plots: Scaler counts as a function of input pulse frequency. Dotted line: A linear line ($y = x$).

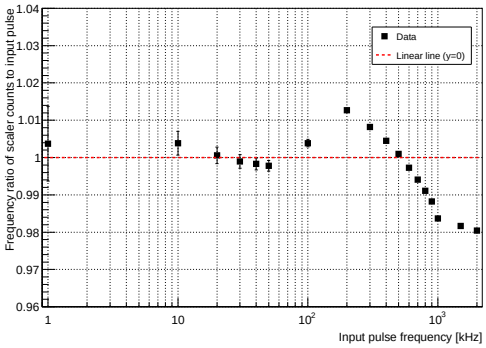

Figure 4.30: Ratio of scaler count frequency to input pulse frequency.

Multi-hit separation

The ability of multi-hit separation as the MHTDC module in the firmware was already measured and it was confirmed that the limitation of multi-hit separation was 7 ns as the width between the trailing edge of the first pulse and the leading edge of the second pulse [48]. Hence, the ability as the NIM-EASIROC module with the new firmware only needs to be measured.

As for the multi-hit separation test, the setup shown in Fig 4.31 is used in order to control delay time between double pulses. In this case the double negative pulse is sent to the capacitor, and the negative charge and positive charge are generated in turn with this order.

The waveform of the injected double-pulse charge to the chip for the multi-hit separation test is shown Fig 4.32. The delay time is decreased down to about 60 ns. The MHTDC distributions with this charge injection are in Fig 4.33. The time width

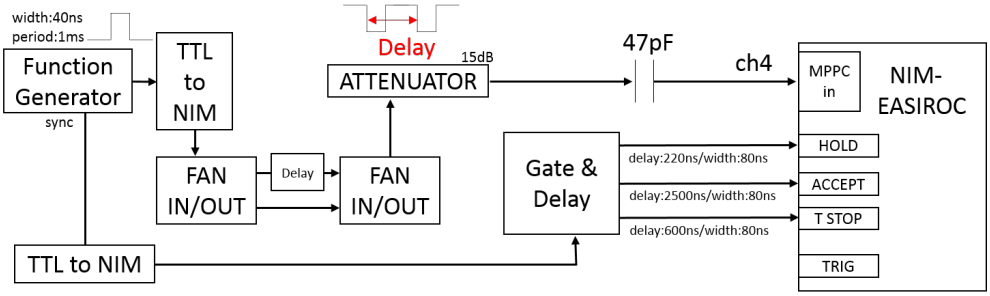

Figure 4.31: The setup for the multi-hit separation measurements.

between the trailing edge of the first signal and the leading edge of the second signal is 16 ns, and it is confirmed that there is no missing edges with this time margin. This separation is small enough compared with the 15 ns shaping time of the fast shaper.

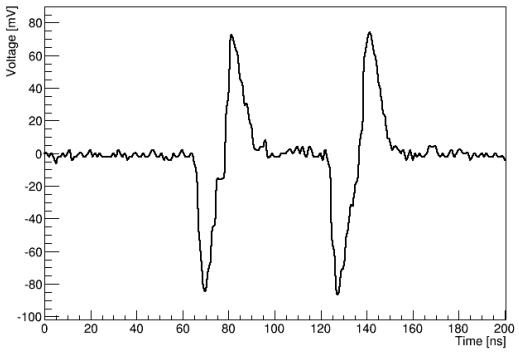

Figure 4.32: The waveform of the injected charges by double pulses.

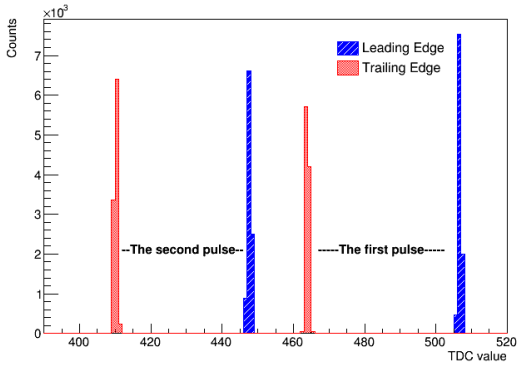

Figure 4.33: The distribution of MHTDC value with double test pulses separated by 60 ns.

4.4.5 The 32-channel arrayed MPPC operation

As the final performance test, the ability to operate a large number of MPPCs at the same time is checked. One 32-channel arrayed MPPC is connected to one of the two chips in the NIM-EASIROC module through 34-pin twist flat cable, and LED light is injected to the MPPCs with 1 kHz. In this case triggers are synchronous with the LED light injection, and the hold signal to the EASIROC chips are delayed to hold the exact peak amplitude of the MPPC signal. Just as simple test measurements, photon counting ability, gain control, and multi-channel operation are checked.

Figure 4.34 shows an example of the distribution of the MPPC signal with overvoltage of around 2 V, and the Gaussians fitting peaks for each number of photo electrons from 0 p.e. to 4 p.e. It is confirmed that photo electron peaks are separated from each other, and it is possible to count the number of photons. Figure 4.35 shows that the gain

changes linearly in accordance with the overvoltage. The MPPC gain is measured as the difference of ADC values between 1 p.e. and 2 p.e., and it is confirmed that the gain is controlled by the InputDAC value of EASIROC.

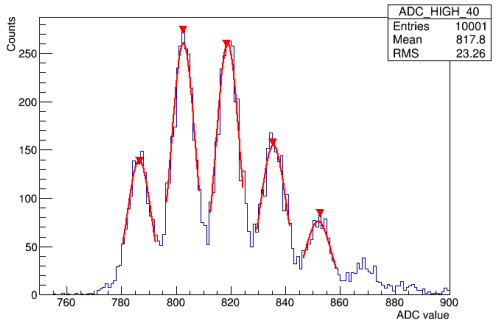

Figure 4.34: MPPC signal distribution with overvoltage of about 2 V, and Gaussians fitting peaks of 0 p.e. to 4 p.e.

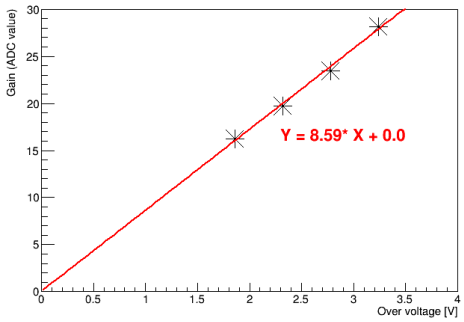

Figure 4.35: MPPC's gain distribution to the overvoltage.

Furthermore, it is confirmed that the EASIROC module is able to control many MPPC channels at the same time. Figure 4.36 shows the ADC distribution for 32 channels of MPPC signals. The pedestal position is adjusted at 750 for the purpose to make the figure easy to be compared between channels. One 32-channel arrayed MPPC is connected to one of two chips on the EASIROC module, which corresponds to channel 0 to 31. The MPPCs are operated at overvoltage of about 3 V. It is observed that there are several peaks of photo electrons from 1 p.e. to 4 p.e. (or 5 p.e.) for each MPPC, and all the 32 channels are correctly operated.

4.5 Summary

In order to implement new functions which are required in the test measurement of MPPC for the WAGASCI detector and requested from users, the firmware of the NIM-EASIROC module has been developed.

All the functions newly added into the firmware are confirmed to work as designed. The selectable logic module, however, needs to be checked more carefully in the future. The test measurements so far are only done with the limited number of inputs and there is no clue that the function works as designed with much more inputs at the same time, or with inputs of the different timings. The performance of the NIM-EASIROC module with the new firmware has also been measured. It is confirmed that performance of the functions required for the MPPC mass test satisfy its requirements, and performance of the other functions is also as expected.

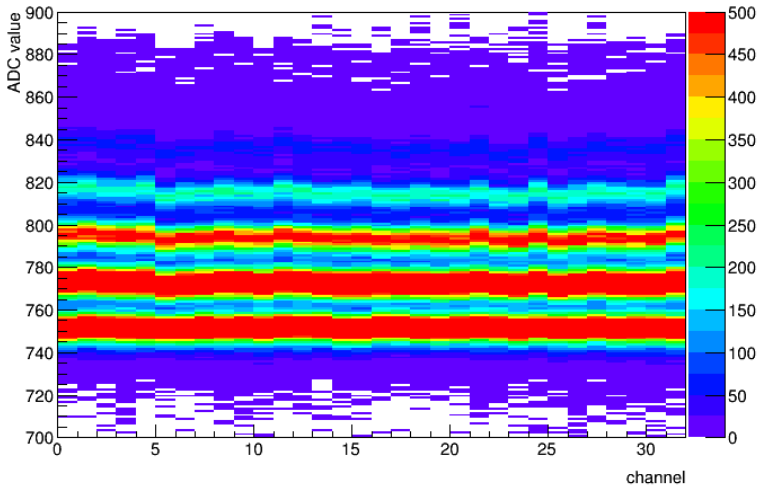

Figure 4.36: MPPC's signal distribution with the overvoltage of about 2V for all the channels on a chip of two, corresponding to channel 32 to 63.

Chapter 5

Development of the WAGASCI electronics with SPIROC2

The electronics of the WAGASCI detector, including the whole DAQ system, are being developed at Laboratoire Leprince-Ringuet (LLR) of l'Ecole polytechnique. The first prototype board has been produced with the two different types of the chip, SPIROC2B/SPIROC2D. In this chapter, the result of the test measurement from October to December 2015 will be discussed.

5.1 New electronics for the WAGASCI detector

The WAGASCI detector adopts the SPIROC2D chip as its front-end electronics. The SPIROC2D chip is a newly developed and will be used for the first time in the WAGASCI detector. For the readout of 7760 MPPCs on the WAGASCI detector, 256 of the SPIROC2D chips are planned to be used. The boards in the WAGASCI electronics are described as follows:

ASU (Active Sensor Unit). The ASU board, as shown in Fig 5.1, has a SPIROC2D chip, and is connected to one 32-channel arrayed MPPC. It also has connections to an Interface board and another ASU via two 50-pin connectors for each.

Interface. The interface board, as shown in Fig 5.2, has connections to four ASUs and a DIF, and transfers signals between the DIF and the four ASUs in parallel. It also has a NIM connection for MPPC bias voltage supply, which is sent to MPPCs through ASUs. Power for the chips such as FPGA on DIF and SPIROC on ASU is also provided through this board.

DIF (Detector InterFace). The DIF board, as shown in Fig 5.3, has an FPGA, which controls the SPIROC chips. It sends DAQ signals and configuration data to the chips, and receives response signals and output data from the chips through the Interface board. The firmware is controlled by the GDCC board through an HDMI connection.

GDCC (Giga Data Concentrator Card). The GDCC board, as shown in Fig 5.4, has HDMI connections of seven DIFs. It has an FPGA, which only works as signal transfer between an Ethernet to a DAQ PC and HDMIs to DIFs. The GDCC board can also function as CCC mode if the corresponding firmware is loaded on the FPGA.

CCC (Clock & Control Card). The CCC board provides all the GDCCs connected to it with clock signals and fast controls.

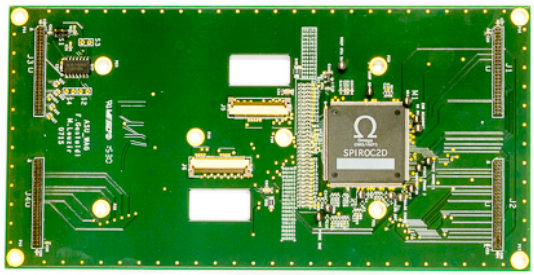

Figure 5.1: Picture of the front side of the ASU board with SPIROC2D.

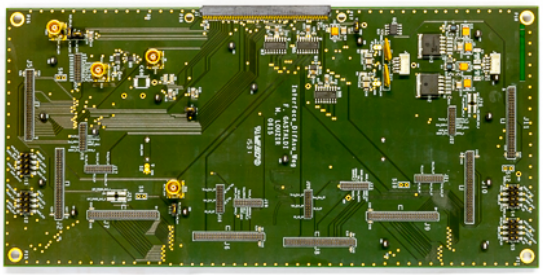

Figure 5.2: Picture of the front side of the Interface board.

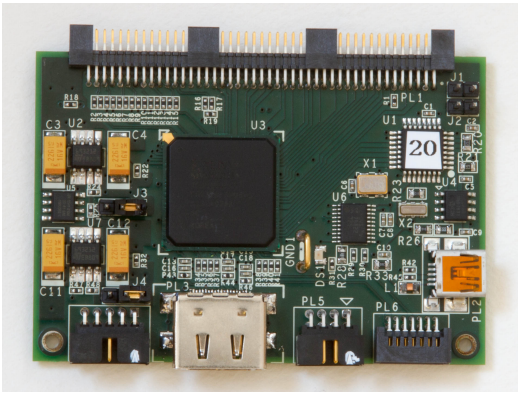

Figure 5.3: Picture of the front side of the DIF board.

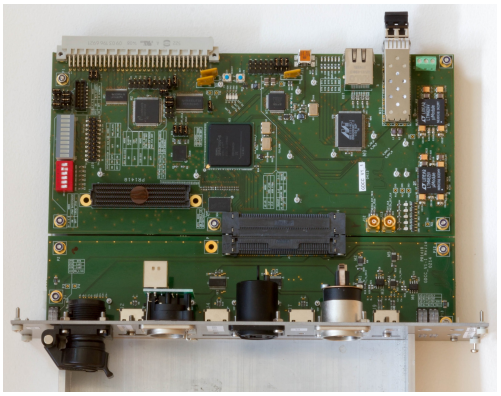

Figure 5.4: Picture of the front side of the GDCC board.

The whole system of the WAGASCI electronics is shown in Fig 5.5. The numbers of boards for the WAGASCI detector are planed as shown in Table 5.1. The DAQ system has been developed in the same way as prototypes of ultra-granular calorimeters for an International Linear Collider (ILC) [59].

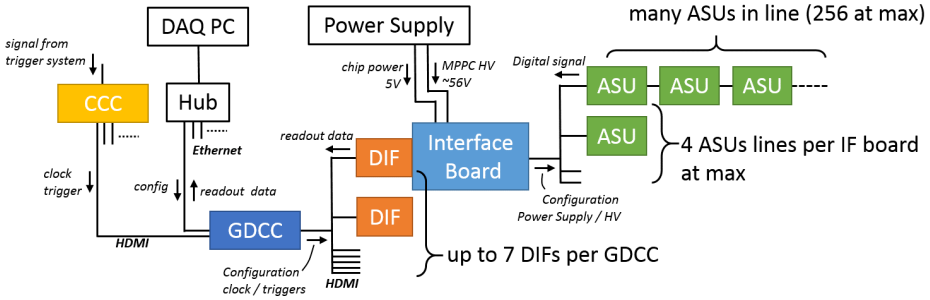

Figure 5.5: The block diagram of the whole system of the WAGASCI electronics.

Table 5.1: The numbers of the WAGASCI electronics boards.

Boards	Central Detector	MRDs	Veto	Total
ASU	160	43	23	226
Interface	8	12	6	26
DIF	8	12	6	26
GDCC	2	2	1	5
CCC	1			1

5.2 SPIROC2

SPIROC is designed as front-end electronics for an ILC prototype hadronic calorimeter with SiPM readout [60]. It has been developed to satisfy requirements such as large dynamic range, low noise, low energy consumption, high precision and large number of readout channels. Table 5.2 shows the basic characteristics of SPIROC. An analog memory array with depth of 16 is embedded on the chip and used to store charge and timing information. A 12-bit Wilkinson ADC digitizes the information and sends the data to 4 kbytes RAM. SPIROC2 is the second iteration which fixes the problems observed on the first version (SPIROC1).

The SPIROC2D chip is a new version of SPIROC2. The former version, SPIROC2B, had wrong behavior on the TDC ramp because of the large dead time due to the multiplexer [61]. In SPIROC2D this problem is solved by implementing a rising and a falling ramp. Although their configurations are done with different numbers of bits, the number and assignment of the pins are compatible between the two versions.

5.2.1 analog part

Figure 5.6 shows the block diagram of the analog parts in SPIROC2. The behavior of the analog parts, such as the high/low gain preamps, slow/fast shapers, discriminator, analog memory, and bias voltage adjustment by 8-bit Input DAC, has already been

Characteristic	Specification
Standard package	CQFP240
Operation voltage	5 V/3.3 V
Power consumption	25 μW per channel (in idle mode)
SiPM gain adjustment	Interanl input 8-bit DAC (0-5 V)
Bi-gain / 12-bit ADC	1 p.e. to 2000 p.e.
Variable shaping time	50 ns to 100 ns
Noise (energy)	pe/noise ratio : 11
TDC	$\sim$100 ps step
Niose (time)	pe/noise ratio on trigger channel : 24
Fast shaper	$\sim$15 ns shaping time
Auto-trigger	on 1/2 p.e.

Table 5.2: SPIROC main characteristics

confirmed through development with EASIROC (Chap 4). In addition, the SPIROC chip is able to obtain timing information, and contains two analog memories with depth of 16 for charge and timing information.

5.2.2 Digital part

SPIROC is equipped with the digital part in the chip. Its readout process has four phases:

Idle phase. In the idle phase, a capture window is open at the first empty data column. This phase saves the power consumption when any other processes are not running.

Acquisition phase. Figure 5.7 (left) shows the diagram of the digital parts relevant to the acquisition phase. At the timing of trigger, information of charge and timing are stored in the analog memory with track and hold circuit and saved in the current data column. When the capture windows are closed, the data column moves to the next at the same time for all the channels. A "bunch crossing", which is a coarse time flag for the triggers, also shifts the column to the next if there is no trigger before the bunch crossing. An external signal is optionally able to erase data in the current column.

Conversion phase. The block diagram related to the conversion phase is shown in Fig 5.7 (right). All the 36 charge and 36 timing in the analog memory are sequentially converted at an ADC with using ramp signals, and the digital data are stored in the 4 kbytes SRAM.

Readout phase. The stored data are transferred out of the chip with a single line, and the analog memory becomes empty after all the data are transferred. If more than one chip are controlled together, a token enabling the data transfer is sent

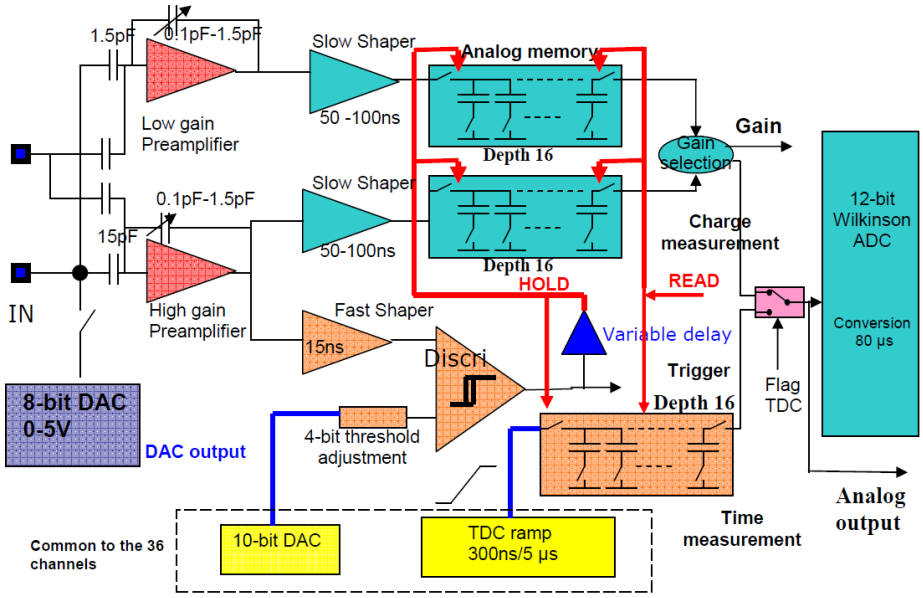

Figure 5.6: The block diagram of the analog part in SPIROC [60].

to the next chip when the data transfer for the first chip is done. The maximum number of chips which can be readout through on serial link is 256.

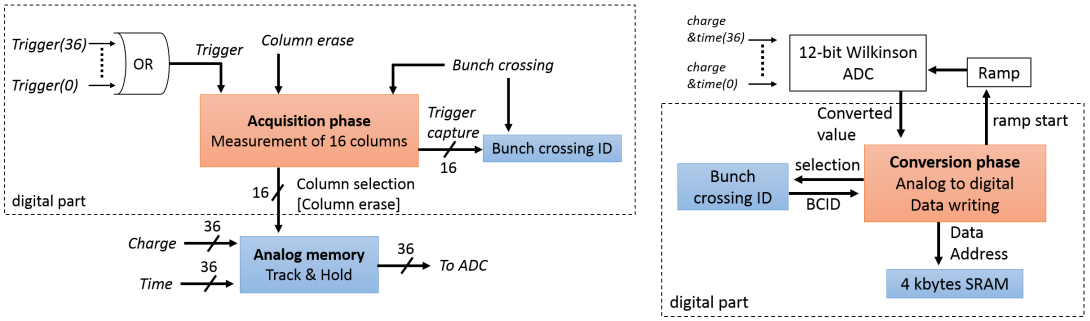

Figure 5.7: The block diagrams of the digital parts in SPIROC. Left: the acquisition phase. Right: the conversion phase.

5.2.3 Slow control and probe registers

The slow control register in SPIROC controls configuration of the chip. It allows to handle a large number of parameters of the chip for both of the analog and digital parts with 929 (1186) bits in the case of SPIROC2B (SPIROC2D). SPIROC2B/D have in common almost all of the slow control registers, but some new parameters are added for

SPIROC2D. For instance, enable/disable registers for LVDS signal receivers of trigger validation, external trigger, and trigger cancel are added.

The probe register enables to probe out both of analog and digital signals inside the chip. It selects a signal and a channel to be probed out by the 952 (992) registers for SPIROC2B (SPIROC2D). SPIROC has the following three probe outputs:

Two digital probe outputs. Digital signals such as value of analog memory, trigger output, validation signal are probed out.

One analog probe output. Analog signals such as preamp signal, fast shaper signal, threshold value, TDC ramp are probed out.

5.3 Link between DAQ and SPIROC

Sequence of phases on the digital parts in SPIROC is controlled by signals from DAQ. SPIROC provides response signals for DAQ. Signals sent from DAQ to SPIROC are start acquisition, start conversion, and start readout, as well as reset and clocks. Signals from SPIROC to DAQ are chip saturation and end readout. Figure 5.8 shows chronograms of the DAQ signals for each case with all the 16 memories full or not full. The DAQ signals control the process in the following order.

1. Reset.
   All the digital part are reset first.

2. Start acquisition.
   The acquisition phase starts and is maintained during this signal.

3. Chip saturation.
   When all the 16 memories become full, the acquisition phase finishes and then the conversion phase starts. When the memories do not become full during the data taking period, the acquisition phase ends and the chip saturation signal is induced to start the conversion phase. This chip saturation signal is maintained during the conversion phase.

4. Start conversion.

5. Start readout.
   As the conversion phase ends with the trailing edge of the chip saturation signal, the readout phase starts with the start readout signal.

6. End readout.

5.4 Development status of the electronics boards

Among the electronics boards necessary for WAGASCI, GDCC and DIF have already been developed. Their functionality was confirmed in the test measurement with an

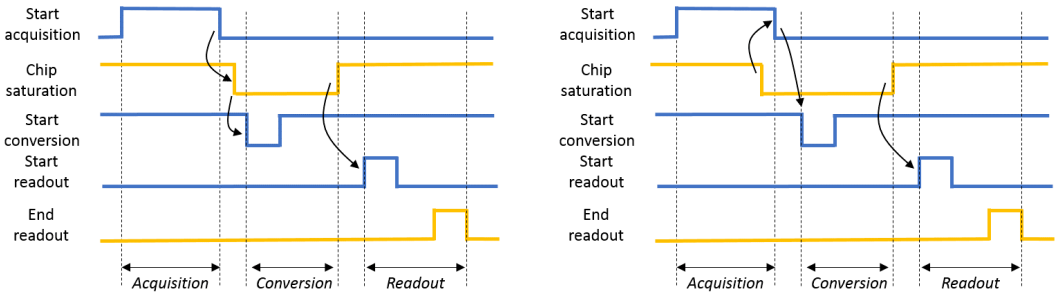

Figure 5.8: The chronogram of the DAQ signals. Left: with the chip not full. Right: with the chip full. Blue lines: Signals from DAQ. Yellow lines: Signals from SPIROC.

evaluation board of SPIROC2B in June 2015. It was also checked that SPIROC2B is able to correctly readout the MPPC signals with ADC (Appendix D.2).

The ASU and Interface boards are required to be newly developed for WAGASCI by summer of 2016. In October 2015, the first prototype of ASU and Interface boards were produced. Three prototype boards of ASU with SPIROC2D were produced, as well as two boards with SPIROC2B as reference boards. The other components of the ASU boards than the SPIROC chip are common in the two versions.

5.5 The first test measurements for the prototype of the WAGASCI electronics with SPIROC2B

First the SPIROC2B prototype boards are tested, because behavior of the SPIROC2B chip was already confirmed while the SPIROC2D chip is totally new. The setup of the test measurement for the prototype electronics with 32-channel arrayed MPPC is shown in Fig 5.9.

In the measurements, one of the GDCCs functions as the CCC mode and sends the DAQ triggers and clock signals to the whole system, in accordance with the spill signal which controls the LED light injection to MPPC and is operated by the software. The structure of the bunches for light injection is adjustable with its width, period, and number of cycles. The LED light is injected through WLS fibers to each channel of MPPCs.

There is two other options instead of a 32-channel arrayed MPPC. One is to use single MPPCs (S13081-050CS(X1)). The single MPPCs are able to be controlled and readout with micro-coaxial cables, which are connected to ASU through a printed circuit board (Fig 5.10). The other is test charge injection. The pulses with the bunch structure are able to be injected to the chip as the test charge through a differentiating circuit.

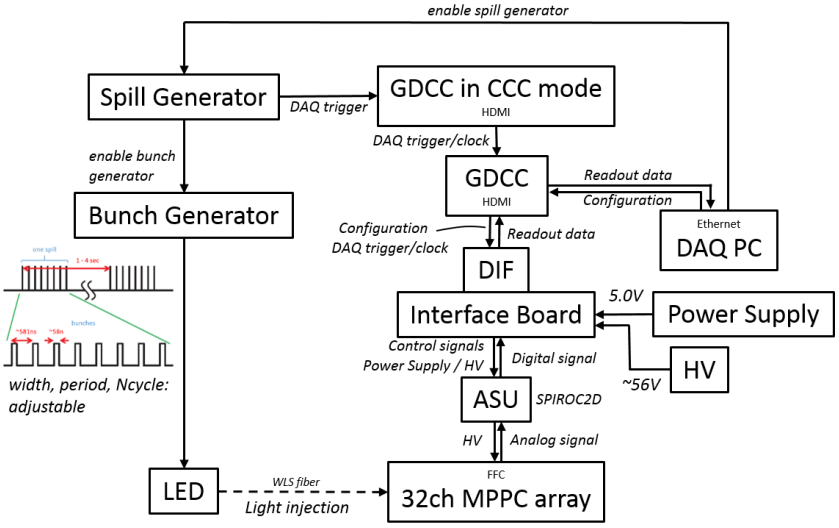

Figure 5.9: The setup of the test measurements for the prototype electronics with 32-channel arrayed MPPC.

5.5.1 DAQ signals

The timing of the signals between DAQ and SPIROC2B is checked first. Figure 5.11 shows a display of the oscilloscope measuring the digital DAQ signals with the test charge injection. In this case the 16 memories are not full. The DAQ signals, such as reset signal ("resetb"), start acquisition ("Startacq"), chip saturation ("ChipSatb"), start conversion ("start_convb"), and end readout ("end_readout"), are correctly sent as the expected timing as described in Sec 5.3. In the readout phase, transmit signal ("TransmitOn1b") is set active and the data ("Dout1b") are sent to the Interface board as expected. It is also confirmed that the validation signal of the triggers ("val_evt") is correctly active during the acquisition phase.

5.5.2 ADC ramp

In order to check the behavior of the SPIROC chip before its digital parts, the ADC ramp inside the SPIROC chip is probed out of the chip.

The amplitude of the ADC ramp signals corresponds to the ADC value, and it must have two different amplitudes for the high gain and low gain preamps in SPIROC. Also, the number of peaks for the ADC ramp signals are expected to be the same as two times of the number of triggers minus one for SPIROC2B. There are high and low gains but the first low gain signal is ignored due to the fluctuation of ADC ramp signal[1].

[1]This fluctuation problem is only for SPIROC2B, and already solved in SPIROC2D. SPIROC2D has the ADC ramp peaks of two times of the number of triggers

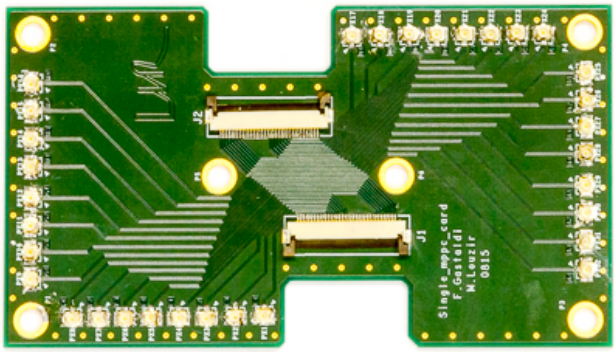

Figure 5.10: The PCB to connect micro-coaxial cables with FFC cables for 32 channels.

Figure 5.12 shows a display of the oscilloscope for the spill, triggers ("OR36"), validation signal ("val_evt"), and ADC ramps with test charge injection. The behavior of ADC ramp in the SPIROC2B chip was incorrect, because the amplitudes were always the same for all and not correlated to the input charge. After the improvement described in Sec 5.5.3, it is confirmed that the ADC ramp behaves correctly as expected.

5.5.3 Efforts to obtain the correct triggers and output data

The OR signal of the 36 discriminator signals is able to be probed out of the chip. This is useful to see if the trigger appears at the corresponding timing to the input signals. However, there had been a lot of difficulties to obtain the correct triggers. The improvements needed to solve the problems on the trigger signal are described in the following.

Decoupling capacitors for the power supply current to the chip

The SPIROC2 chip has a large number of inputs for the bias voltage and current, and each one of them is connected to the ground through decoupling capacitors. Although all these decoupling capacitors are designed in the schematic to be soldered, the prototype boards had been produced without any of the decoupling capacitors. It is confirmed that the whole system of the SPIROC chip behaves unstably without the decoupling capacitors. For the OR signal of the triggers, for instance, the base level of the signal occasionally stays at the ground (0 V) as shown in Fig 5.17, while it must always stay at high level (3.3 V). This random behavior disappears after all the decoupling capacitors are soldered on the board.

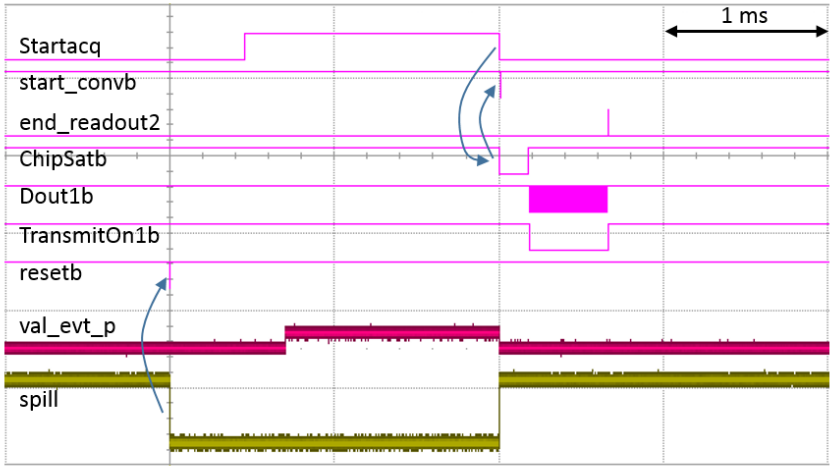

Figure 5.11: The display of oscilloscope for the digital signals from the DAQ and the response from SPIROC2B.

External trigger

Although the SPIROC chip is mainly operated with the auto-trigger mode by the discriminator signals, there is also the external trigger mode where all the triggers are issued with the external LVDS signal. Figure 5.14 shows the block diagram for the flow from the MPPC input to the trigger signal, including the external trigger. A register is supposed to be set for ignoring the external trigger. However, when the two LVDS inputs of external trigger are open an unexpected single pulse has been observed on the trigger signal at the beginning of the validation signal. In this case no trigger corresponding to the input appears. It means that the external trigger is always active and disables the auto-trigger.

Thus, the lower level signal of the LVDS external trigger is fixed at a constant voltage of around 1 V in oder to disable the external trigger for sure. After the modification, the strange single pulse at the beginning of validation signal disappears and the triggers corresponding to the input charge are observed.

Noises due to unstable grounding

Even after the external trigger problem was fixed, there were noises on the trigger signal at the beginning of the validation signal as shown in Fig 5.15. Due to these noises, all the 16 triggers appear immediately after the validation signal. Thus, the analog memory becomes full and has no more space for the correct triggers. It seemed that the whole system was too sensitive to the grounding. For example, when the PCB for the connection between the micro-coaxial cables and FFC cables is used, the noises on the trigger signal appeared as shown in Fig 5.15. A possible explanation for this is that

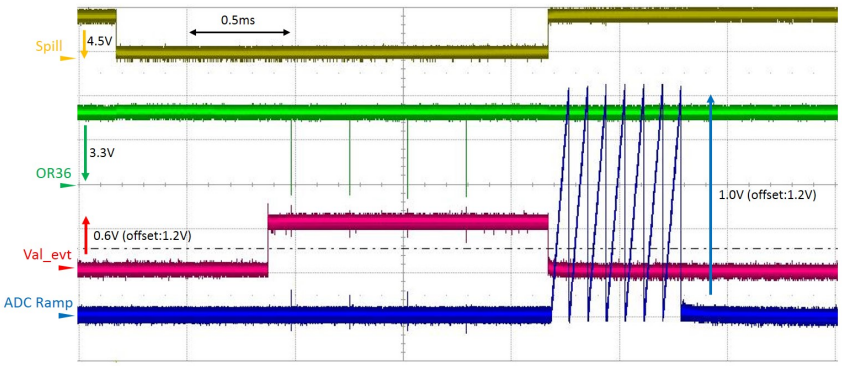

Figure 5.12: The display of oscilloscope for wrong behavior of ADC ramp.

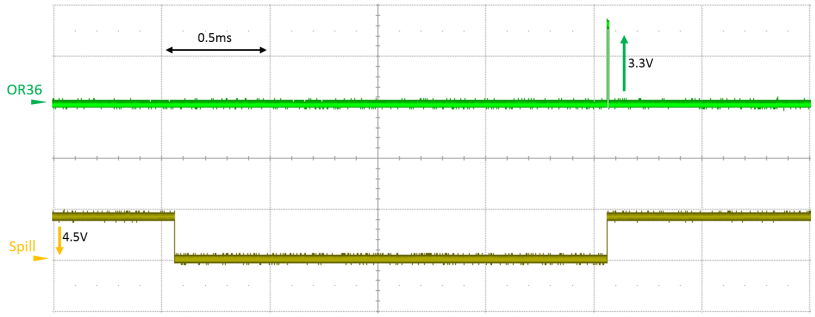

Figure 5.13: The display of oscilloscope for the trigger signal, the ground level of which is at 0 V unexpectedly.

there is no ground line in the 36-pin FFC cables between the ASU and PCB and the relative ground levels of these two boards are unstable.

In order to temporarily solve the problem, the micro-coaxial cable is cut and directly soldered to the input and ground on the ASU board, instead of using the PCB. Since then, all the noises on the trigger signals are gone and it becomes able to observe the triggers at the corresponding timing to the input signals.

Probe register

SPIROC has a pin named "select." Depending on the signal level of the select pin, the destination of chip configuration data is switched between the slow control register and the probe register. The position of this pin has been changed during the chip development, but the firmware on DIF did not take into account the change and had the wrong connection. The problem on SPIROC2B is that there is no reset function

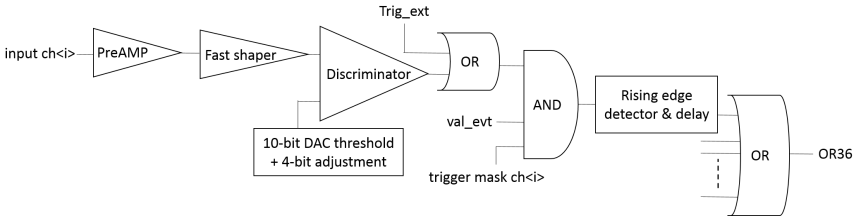

Figure 5.14: The block diagram from the input to "OR36" including the external trigger (SPIROC2B).

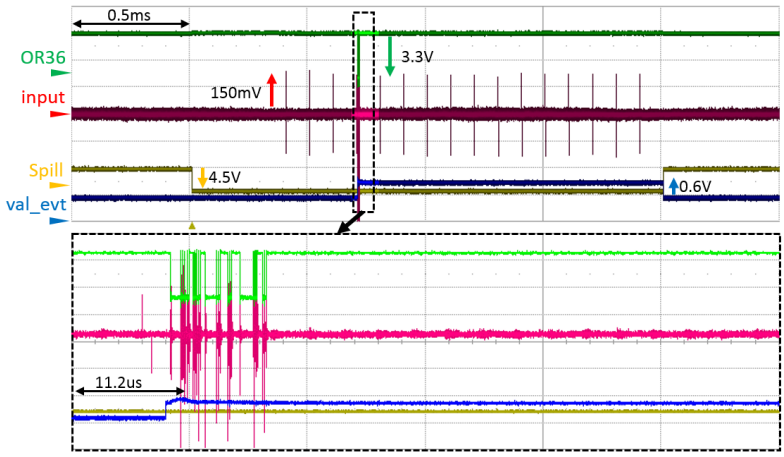

Figure 5.15: The display of oscilloscope for the OR signal of the discriminator signals ("OR36"), injected charge ("input"), spill signal, and validation signal ("val_evt").

for the probe register. Hence once it is unexpectedly configured it keeps the state and might contain the unexpected shortcut in the chip.

An example of the unexpected signal from the digital probe is shown in Fig 5.16. The digital probe output must stay at ground level when nothing is configured, but in this case the 2.5MHz clock signal is probed out during the acquisition phase. In order to avoid the problem, the configuration data with all zero values is sent to the probe register. Then the problem is solved, and the digital probe output stays at the ground level.

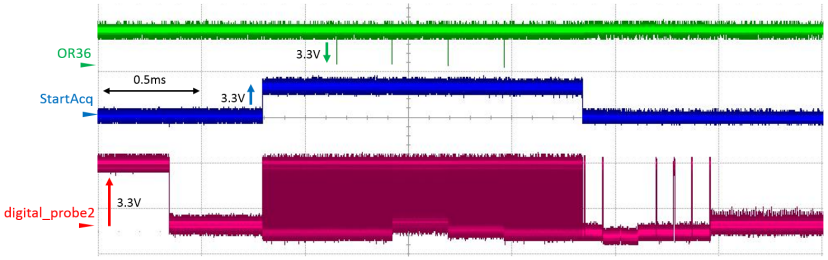

Figure 5.16: The display of oscilloscope for the unexpected signal of the digital probe.

Slow control registers for TDC

Even after the triggers started to be observed at the correct timing, the output ADC value with the charge injection was always zero. This problem has been solved by turning off the two registers for TDC: one is for disabling the TDC and the other is for disabling the external TDC flag. As either one of them was turned on, the ADC ramp signals were always observed with the same height, although they were expected with two different heights. A possible explanation is that the TDC registers made a wrong shortcut on the line from the input to ADC ramp and the digital part did not receive the correct signal. It must also be noted that SPIROC2B has been known to have a problem on the TDC.

Expected behaviors

After all the efforts to obtain the correct triggers and output data, behavior of the trigger signals and ADC ramps is observed as expected as shown in Fig 5.17. Then, it becomes able to measure basic functionality of the WAGASCI electronics.

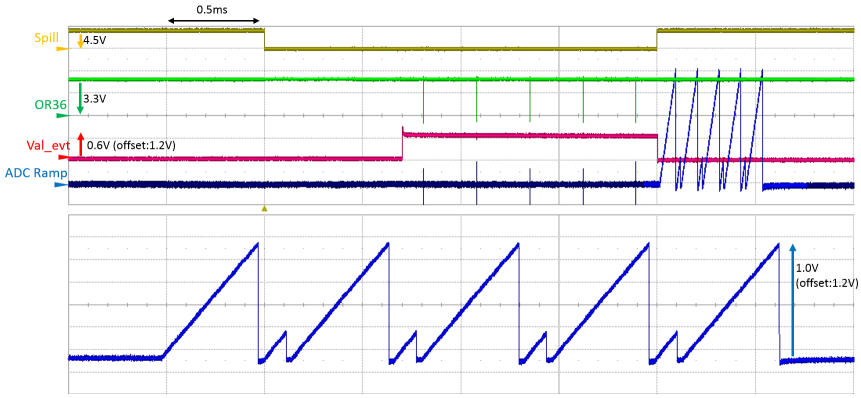

Figure 5.17: The display of oscilloscope for the signal of ADC ramp corresponding to high gain and low gain.

5.5.4 Readout of the MPPC signal

After improvement of the stability of the the whole system, a test with the real MPPC signal was performed. The setup is the same as shown in Fig 5.9, but a single MPPC is used instead of 32-channel arrayed MPPC. The micro-coaxial cable for the MPPC connection is cut and directly soldered on the input and the ground of the ASU board. The MPPC is operated with around the overvoltage of 2.5 V. The LED light is injected to the MPPC with the three bunches per spill, where the frequency of the bunches is 3.7 kHz and that of the spills is 10 Hz.

Figure 5.18 shows the ADC distributions of the MPPC signal and the pedestal. In the MPPC signal, the photo electrons are observed from 2 p.e. to 7 p.e. (or 8 p.e.). It shows the photon counting ability as expected. Figure 5.19 shows the bunch crossing IDs. The bunch crossing IDs are incremented at the exact timing for each of the three triggers with one bin or two. During the acquisition phase, dark noises of the MPPC are observed. The rate becomes small just after the three LED light injection because of the MPPC's saturation as expected. All the data means that the SPIROC2B prototype electronics are applicable to the MPPC readout.

Then, the number of bunches is increased up to 70, and the frequency of bunches is increased up to 25 kHz, in order to fill all the 16 columns within the acquisition phase. It is confirmed that the distribution of photo electrons can be observed at all the 16 columns, except for the first column ignored.

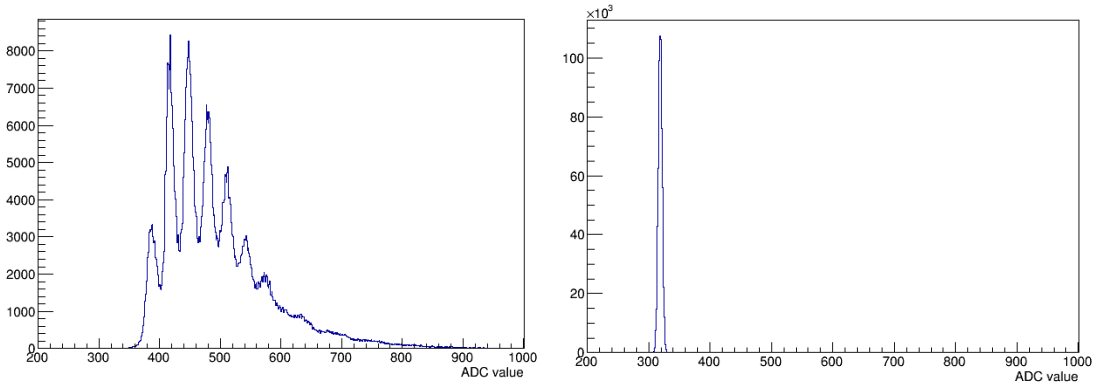

Figure 5.18: The ADC distribution for the MPPC test measurement with the SPIROC2B prototype boards. Left: MPPC signals. Right: Pedestal signals.

5.6 The WAGASCI electronics with SPIROC2D

5.6.1 Unstable start of data acquisition

When starting the test measurement of the SPIROC2D boards with the same setup as that of SPIROC2B boards, it was not possible to readout the MPPC signal nor

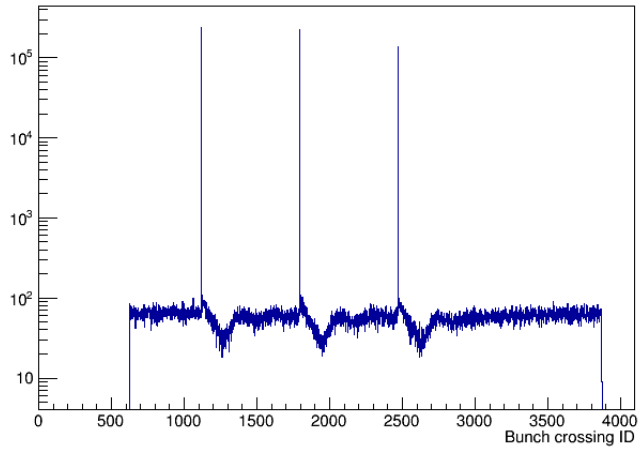

Figure 5.19: BCID distribution with three bunches.

the test charge injection. The data acquisition was unstable. For example, no triggers were observed at first just after data acquisition starts, and about one minutes later the whole chip started working and triggers started to be observed. In this case, the output data did not contain the corresponding values to the charge injection although the triggers were observed at the correct timing.

There is an analog bias input for the SPIROC2B/D chip, in order to provide the preamp input and output stage with minimum bias current. This input is connected to the ground through a 10 kΩ resistor, and this connection is indispensable for the SPIROC2B operation. For the SPIROC2D operation, however, this connection is not required, and the current flow to the preamp inside the chip produces the unstable state of the preamp. Removing the 10 kΩ resister from the ASU board with SPIROC2D, the problem of unstable start of the data acquisition was solved.

5.6.2 Future prospects

The test measurements of functionality for the WAGASCI electronics with SPIROC2D becomes possible now. Starting with the simple readout of MPPC signals, it is also required to check the possibility of readout with the bunch structure for WAGASCI. These measurements will start at beginning of 2016.

5.7 Summary & future plans

As new electronics for the WAGASCI detector to readout 7760 MPPCs, the electronics boards with SPIROC2D have been developed at LLR. In October 2015, the prototype boards with SPIROC2B/D have been produced and their test measurements have been done. After improvement of the stability of the whole system, it is confirmed that the SPIROC2B prototype board is able to readout the MPPC signal with the bunch structure, where the frequency of the bunch is 3.7 kHz and that of the spill

is 10 Hz. For the SPIROC2D boards, its unstable data acquisition is now solved. It becomes possible to test the SPIROC2D boards with MPPCs.

At the beginning of the year 2016, the readout ability of the SPIROC2D prototype board will be tested. If it would be confirmed that the board could readout the photoelectrons, the second prototype boards will be produced in accordance with the research and development in this document, including the update of the DIF firmware. The final version will be produced during the summer of 2016 and will be installed into the WAGASCI detector.

Chapter 6

Summary

In order to reduce the current dominant systematic uncertainty in the T2K neutrino oscillation analysis, WAGASCI will measure the neutrino charged current cross section ratio between water and hydrocarbon. Currently the detector design is almost done. The cross section ratio is expected to be measured with a total uncertainty of 3%. The WAGASCI project will start the physics data taking in the autumn 2016.

For anti-neutrino cross section measurement in WAGASCI, discrimination of the contamination of neutrino background events is important. An option to install the magnetized downstream MRD instead of the current non-magnetized downstream MRD is studied to reduce the contamination by charge identification of muons from neutrino interactions. A simple method to identify charge by fitting muon tracks with a quadratic function is established. The efficiency to correctly select anti-neutrino events is expected to be 89%, and the neutrino background contamination is expected to be reduced to 3%. The number of anti-neutrino charged current events is expected to be 1.4×10^4 with 10^{21} POT, and its purity is 97%. Hence, precise measurement of anti-neutrino cross section with the same level as the neutrino cross section measurement is promising.

The mass test of MPPCs used in WAGASCI adopts the NIM EASIROC module as the readout electronics. To implement some new functions required for the mass test, the firmware on the module is updated. The performance of the NIM EASIROC module with the updated firmware is tested. All the newly implemented functions are checked to work as designed. Linearity of ADC to input charge is confirmed. Time resolution is measured as 0.53 ns. The precision of the scaler function is 2% up to 2 MHz. Simultaneous operation of 32-channel MPPCs is confirmed to be possible. All the performance satisfies requirements for the MPPC mass test measurement.

WAGASCI will use new electronics with SPIROC2D to readout MPPCs in the detector. The first prototype boards of the new electronics were produced with SPIROC2B and SPIROC2D in October 2015. The MPPC readout with the SPIROC2B prototype board is established. For the SPIROC2D boards, the problem on unstable data acquisition is solved and test measurement will start soon.

Acknowledgment

I would like to express my deepest gratitude to my supervisor, Prof. Yokoyama, who offered continuing support and constant encouragement. I also owe a very important debt to all colleagues in the T2K experiment and the WAGASCI experiment, and members in Aihara/Yokoyama group in the University of Tokyo. They gave me all the opportunity to gain experience. Finally, I would like to thank Advanced Leading Graduate Course for Photon Science (ALPS) at the University of Tokyo for a grant that made it possible to complete this study.

Appendix A

Calculations for the thickness of the first iron plate in the magnetized downstream MRD

The thickness of the first iron plate in the magnetized downstream MRD is constrained by simple calculation of charge identification efficiency and muon rang in iron. The calculations determined the thickness as 9 cm, and the thickness is adopted in the current configuration discussed in Sec 3.4.

A.1 Charge identification

As a charged particle passes through the magnetized iron, the direction of motion is varied by the magnetic force for a particular direction. However, at the same time, the particle is also affected by multiple coulomb scattering. Multiple scattering direction is totally random, so that it causes the inefficiency of the charge identification as shown in Fig A.1.

Suppose a negative muon comes perpendicularly to a iron plate magnetized uniformly and bent by the magnetic field as shown in Fig A.2. The radius of the orbit, R, is determined with the strength of the magnetic field, B, and the muon momentum, p:

$$R\ [\mathrm{m}] = \frac{p\ [\mathrm{GeV/c}]}{0.3 \times B\ [\mathrm{Tesla}]}. \tag{A.1}$$

The scattering angle, θ, is calculated as

$$\sin\theta = \frac{X}{R} = \frac{0.3 \times B\ [\mathrm{Tesla}] \times X\ [\mathrm{m}]}{p\ [\mathrm{GeV/c}]}. \tag{A.2}$$

The scattering angle due to multiple coulomb scattering is calculated [16] as

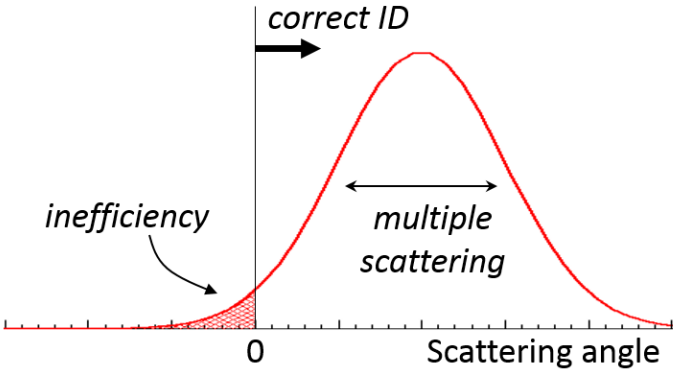

Figure A.1: Concept of the charge identification.

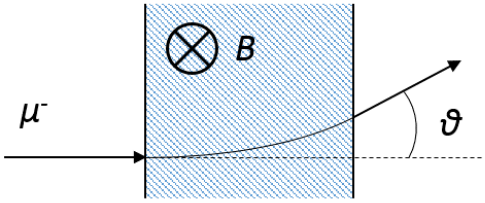

Figure A.2: Muon is bent by the magnetic field.

$$\sqrt{\theta^2_{\rm proj}} = \frac{13.6\ z}{p\ [\mathrm{MeV/c}] \times \beta c}\sqrt{\frac{X}{X_0}}\left[1 + 0.038 \log_{10}\left(\frac{X}{X_0}\right)\right]. \tag{A.3}$$

Here p, βc, and z are the momentum, velocity, and charge number of the incident particle, and X/X_0 is the thickness of the scattering medium in radiation lengths. The radiation length for iron is 1.757 cm.

The scattering angles by the magnetic field and multiple coulomb scattering are calculated with different iron thickness of 3 cm, 6 cm and 9 cm, as shown in Fig A.3 and A.4, respectively. For the case with the iron thickness of 3 cm and 6 cm, the RMS of the multiple scattering is equal to or larger than the scattering angle by the magnetic field.

Figure A.5 shows the efficiency to correctly identify the charge sign, which is calculated assuming an exact gaussian distribution whose dispersion is the multiple scattering angle (Eq A.3), and mean value is the scattering angle due to the magnetic field (Eq A.2). The efficiency to correctly identify the particle charge is no more than 84% (77%) for the case with 6(3)-cm-thick iron. For the 9-cm-thick magnetized iron plate, the charge identification efficiency is expected to be around 89% for muon momentum larger than 500 MeV, and 86% to 88% down to 200 MeV. Although these values do not reach the requirements, track fitting would improve the efficiency as discussed in Sec 3.5.

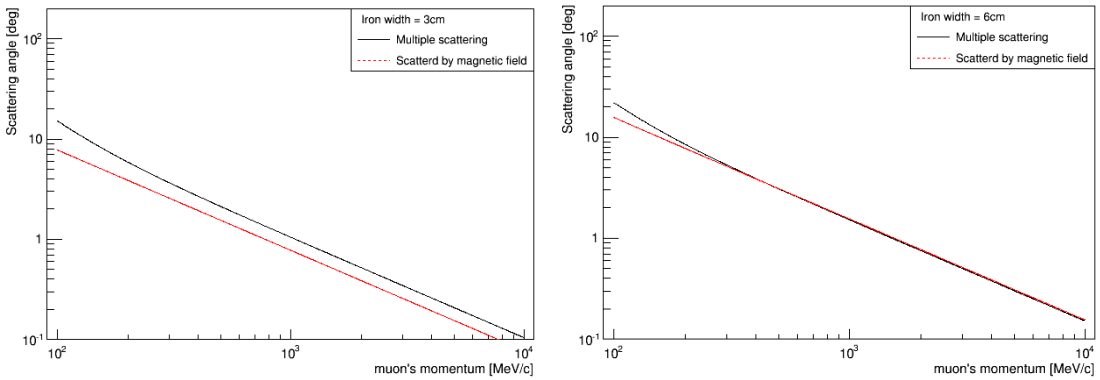

Figure A.3: Scattering angles by the magnetic field and multiple scattering. Left: Fe = 3cm. Right: Fe = 6cm.

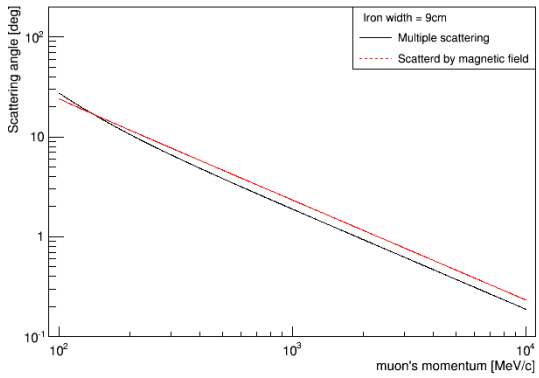

Figure A.4: Scattering angles by the magnetic field and multiple scattering. Fe = 9cm.

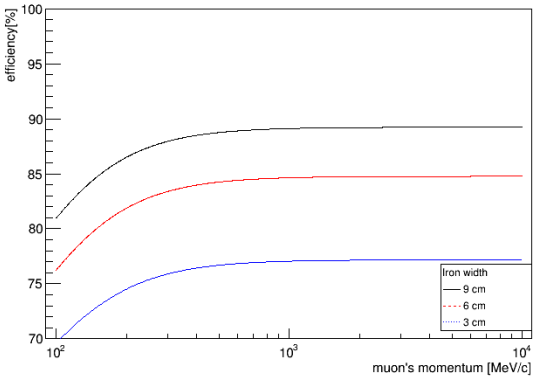

Figure A.5: The charge identification efficiency.

A.2 Muon range in iron

In order to measure the energy of muons, the range of the charged particles in iron needs to be taken into account for the design of the MRDs. The range of charged particles, such as muon, pion, and proton, is estimated by the electric energy loss in the material for relativistic charged heavy particles, which is well described by the Bethe equation [16],

$$\left\langle -\frac{\mathrm{d}E}{\mathrm{d}x} \right\rangle = \frac{Kz^2 Z}{\beta^2 A}\left[\frac{1}{2}\ln\frac{2m_e c^2\beta^2\gamma^2 W_{\max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right]. \quad \text{(A.4)}$$

$$K = 4\pi N_A r_e^2 m_e c^2 = 0.307075 \ [\mathrm{MeV\ mol^{-1}\ cm^2}]$$

I : mean excitation energy

z : charge number of incident particle

Z : atomic number of absorber

A : atomic mass of absorber

$W_{\max}$: Maximum energy transfer in a single collision

It describes the mean energy loss in the region of $\beta\gamma$ from 0.1 to 1000 for intermediate atomic number materials with an accuracy of a few percents. Here the maximum energy transfer in a single collision, $W_{\max}$, is calculated as

$$W_{\max} = \frac{2m_e c^2 \beta^2 \gamma^2}{1 + 2\gamma m_e/M + (m_e/M)^2}, \tag{A.5}$$

with mass of the incident particle as M. The values of I, Z, and A for iron are 286.0 eV, 26, and 55.845, respectively.

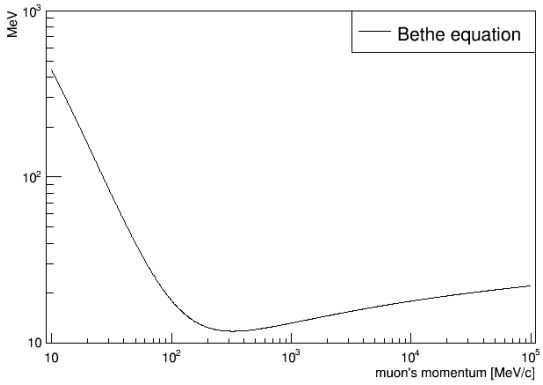

Figure A.6: The stopping power of muon in iron.

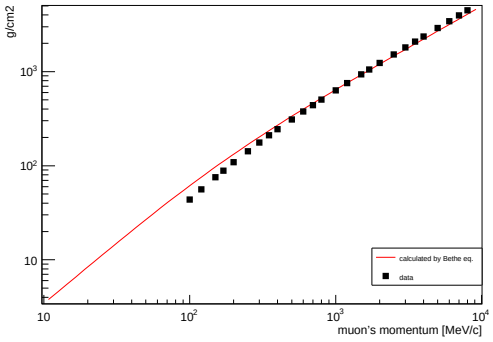

Figure A.7: The calculated range of muon in iron, and data.

Figure A.6 shows the stopping power of muon in iron which is calculated by the Bethe equation, Eq A.4. Here the density of iron is 7.87 g·cm^{-3}. The density-effect correction term, $\delta(\beta\gamma)$, is ignored because the energy of muon is relatively small for the correction. The range of muons in iron, R, can be estimated by the Bethe equation,

$$R = \int_{E_{\min}}^{E^0_{\mathrm{kin}}} \left\langle -\frac{\mathrm{d}E}{\mathrm{d}x} \right\rangle^{-1} \mathrm{d}E_{\mathrm{kin}}. \tag{A.6}$$

Here the stopping power of muon in iron is integrated from the minimum energy applicable to the Bethe equation, $E_{\min}$ (5 MeV is set here), to the initial kinetic energy of muon, E^0_{kin}. Additional effect for the lower energy than $E_{\min}$ must be taken into account for the precise calculation, while the effect is not significantly large. The calculation without this additional effect is consistent with the measured data [62] within 20% from 200 MeV to 10 GeV, as shown in Fig A.7, thus the effect is ignored here. Figure A.8 shows the ranges of muon, charged pion, and proton, in iron and aluminum.

From the $\bar{\nu}_\mu$ interaction in the WAGASCI central detector. About 95% of the protons and 80% of the charged pions from the $\bar{\nu}_\mu$ interaction in the central detector have

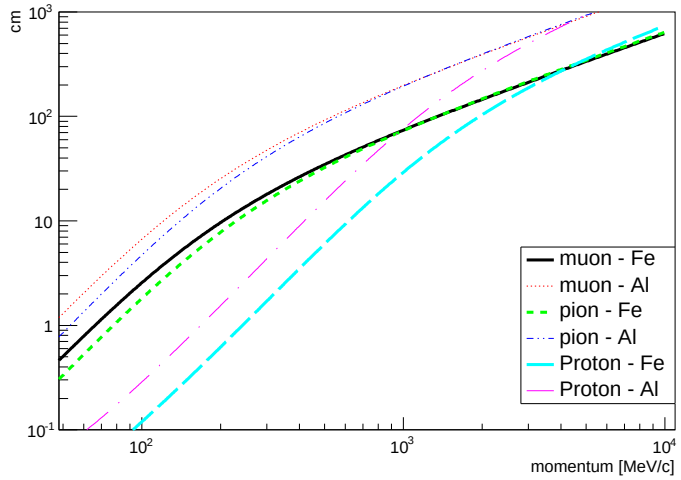

Figure A.8: Ranges of the charged particles in iron and in aluminum.

shorter range than 9 cm with its initial energy. The ranges for 93% of the muons are longer than 9 cm, therefore the 9-cm-thick iron plate satisfies the requirements as the first plane in the downstream MRD to stop other charged particles than muon.

Appendix B

Aluminum coils in the magnetized downstream MRD

In order to evaluate the effect of aluminum coils, a structure with aluminum is implemented into the GEANT4 detector, Fig B.1. 5-mm-thick aluminum is wound with the individual steel plate for 2 m width. Comparing the ranges of muon in aluminum

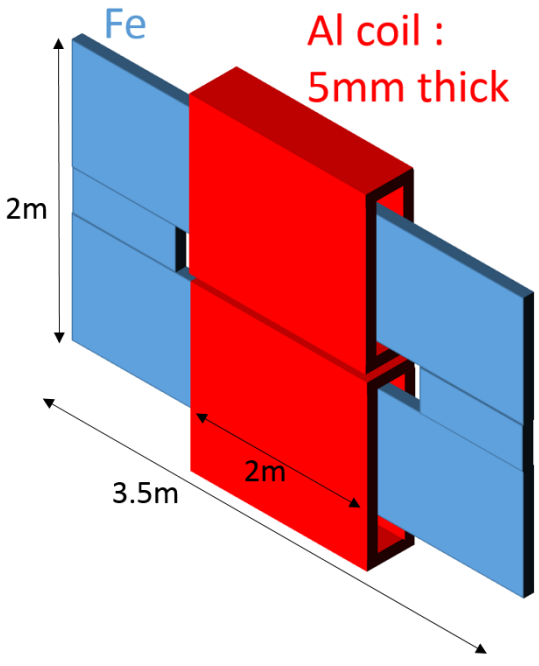

Figure B.1: How to implement aluminum coils into GEANT

and iron, Fig A.8, almost all the difference come from the difference in density. The

density of aluminum is 2.7 times smaller than that of iron. If a 5-mm-thick aluminum plate wind around a 3-cm-thick iron plate, the total range in the view of muon increases by 12%. That difference affects the distribution of the neutrino energy when requiring muons to stop within the downstream MRD, Fig B.2, B.3. In this study the first iron plate was still kept 6 cm. The whole distribution is shifted to higher energy, because it becomes a bit easier with the aluminum structure to stop charged particles in the downstream MRD and particles with small energy get harder to penetrate the first iron plate. The number of reconstructed muon tracks are increased by 20% around at neutrino energy of 1.6-1.8 GeV but decreased by 8% around at 0.4-0.5 GeV.

The ability of charge identification is also compared with the configurations with/without aluminum structures. As the result, the efficiencies to correctly select $\bar{\nu}_\mu$ events are the same as each other within 1%, and the contaminations of wrong sign neutrino events are the same within 5%.

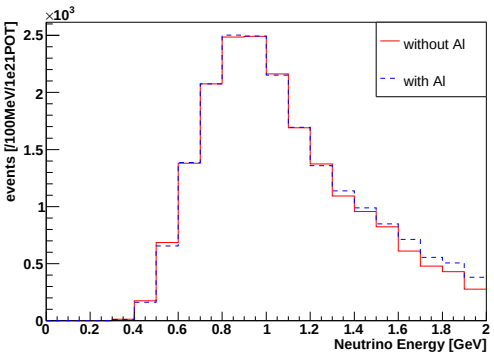

Figure B.2: Neutrino energy distribution with/without aluminum structure.

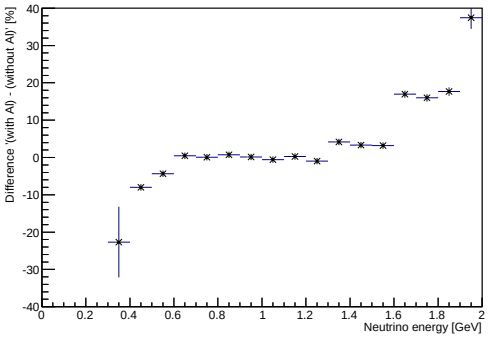

Figure B.3: Difference of the neutrino events between with/without aluminum structure.

Appendix C

Timing analysis for the firmware of EASIROC

The signal timing inside the FPGA is analyzed in terms of setup time and hold time. Figure C.1 shows the data arrival time and clock arrival time between two flip-flops, a sender and a receiver. Figure C.2 shows the concept of setup analysis and hold analysis. Setup time and hold time are explained in the followings:

Setup time For a flip-flop to capture data at the same time when clock signal reaches at its clock pin, its input data is required to arrive the flip-flop a time before the positive clock edge. The time is called setup time.

Hold time For the same purpose, its input data should not change for a time after the positive clock edge, and otherwise the positive clock edge capture the next data. The time is called hold time.

Data arrival time is a data transfer time from a common clock source sending the data to the receiver flip-flop though the sender flip-flop. Clock arrival time is a clock transfer time from the common clock source to the receiver clock. The clock arrival times are different for the setup analysis and the hold analysis. To correctly operate the circuit, the data arrive time must satisfy the following relations compared with data required time:

$$\begin{aligned} &\langle\text{Data arrival time}\rangle < \langle\text{Setup data required time}\rangle \\ &\quad = \langle\text{Clock arrival time}\rangle - \langle\text{Setup time}\rangle - \langle\text{Setup clock skew}\rangle \qquad \text{(C.1)} \\ &\langle\text{Data arrival time}\rangle < \langle\text{Hold data required time}\rangle \\ &\quad = \langle\text{Clock arrival time}\rangle + \langle\text{Hold time}\rangle + \langle\text{Hold clock skew}\rangle \qquad \text{(C.2)} \end{aligned}$$

These timings are evaluated with slack values, are calculated as:

$$\begin{aligned} \langle\text{Setup slack}\rangle &= \langle\text{Setup data required time}\rangle - \langle\text{Data arrival time}\rangle \qquad \text{(C.3)} \\ \langle\text{Hold slack}\rangle &= \langle\text{Data arrival time}\rangle - \langle\text{Hold data arrival time}\rangle \qquad \text{(C.4)} \end{aligned}$$

The negative value of slack means the timing violation. The worst slack values for the new firmware are evaluated for setup as 0.036 ns and for hold as 0.053 ns. It is confirmed that there is no timing violation with the current firmware design.

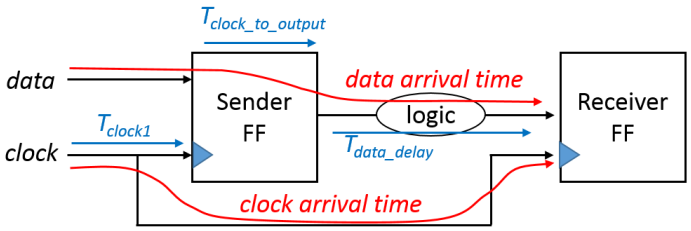

Figure C.1: Data arrival time and clock arrival time.

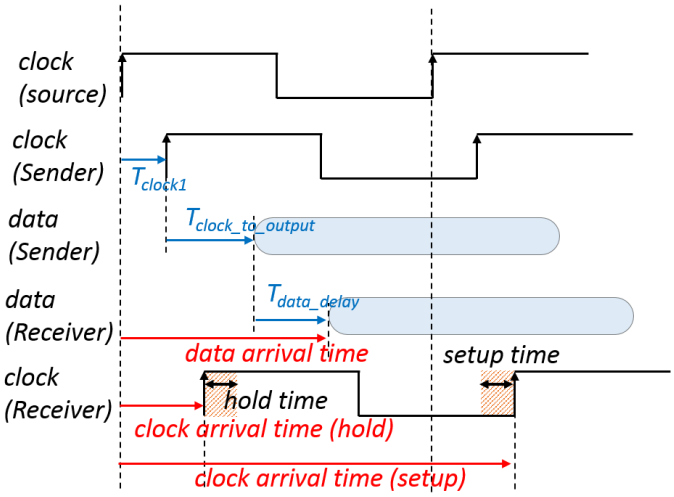

Figure C.2: Setup analysis and hold analysis.

Appendix D

More information of the prototype electronics with SPIROC2B

D.1 Other miner problems of the prototype electronics with SPIROC2B

Buffer chip on the interface board There were wrong behavior on "chip_sat". Originally the problem is that the chip is mounted on the wrong orientation. Now it's temporarily removed.

LVDS validation signal's wrong polarity The firmware had the wrong positions of "val_evt" signal, that is the positive and negative poles are flipped.

Bias voltage for analog parts and digital parts As separating the bias voltage supply into analog part and digital part, the noise on the whole system seems decreased.

D.2 The readout of the MPPC signals with the SPIROC2B evaluation board

Before starting the performance test of the prototype boards, the response of the SPIROC2B chip to MPPC signals is test with the evaluation boards. The setups are the same as the setup for the prototype boards, as written in the Fig 5.9. It is observed that SPRIOC2B is able to count the number of photo electrons from the MPPC, as Fig D.1, but at the same time it is sensitive to the unstable ground level because the ADC distribution is disturbed by noises with the shape of spikes, as shown in Fig D.2 by removing the ground connections between modules.

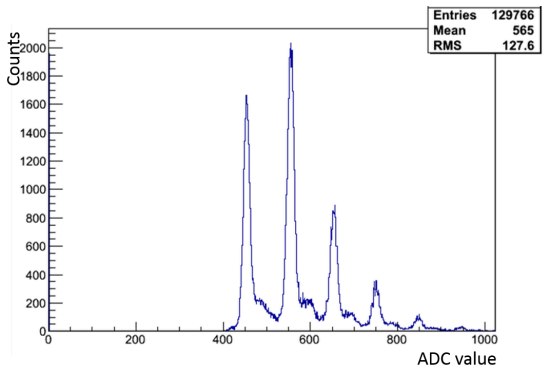

Figure D.1: The ADC distribution of SPIROC2B with the evaluation boards for the light injection to MPPC.

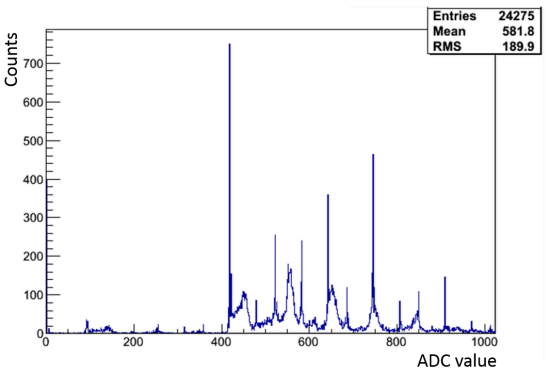

Figure D.2: The ADC distribution with the evaluation boards for the MPPC signals, without the ground connection between modules.

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